WAI 2025 Ningbo, China November 5 – 7, 2025

IEEE wai 2025

2025 International Workshop on
Advanced Interconnects
Ningbo, China

WAI 2025

November 5 – 7, 2025

Advance program

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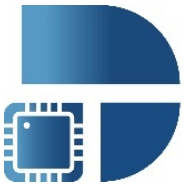

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INVITATION FROM THE GENERAL CHAIR

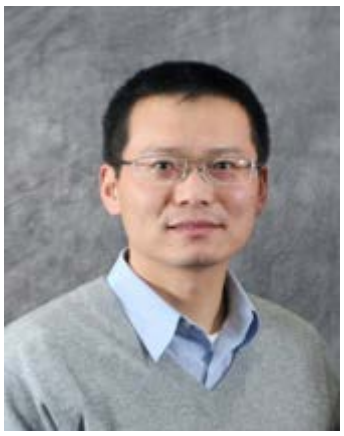
Dear Colleagues and Friends,

Welcome to WAI 2025! This is the second International Work shop on advanced interconnects. The scope of this workshop includes, but is not limited to signal integrity and power integrity of an electronic system and its components including advanced interconnects, integrated circuits, IC packages, printed circuit boards, cables, connectors, as well as other relevant electronic and microelectronic components, and signal integrity/ power integrity co-design.

WAI 2025 also welcomes all papers or presentations related but not limited to electromagnetic environments; interference control; EMC and EMI modeling; high power electromagnetics; EMC standards, methods of EMC measurements; computational electromagnetics and signal and power integrity, as applied or directly related to EMC problems; transmission lines; electrostatic discharge and lightning effects; EMC in wireless and optical technologies; EMC in printed circuit board and system design; radio-frequency interference problems; artificial intelligence-assisted EMC/SI/PI design methodologies.

We would like to express our thanks to our coorganizers, sponsors, contributors and all of the attendees for your hard work and effort! Our best wishes are to all WAI 2025 attendees, and we hope all of you enjoy your time in Ningo and have a great time!

WAI 2025 General Chairs



Jun Fan, IEEE Fellow

Qiushi Professor, Zhejiang University

Er-Ping Li, IEEE Fellow

Qiushi Chair Professor, Zhejiang University

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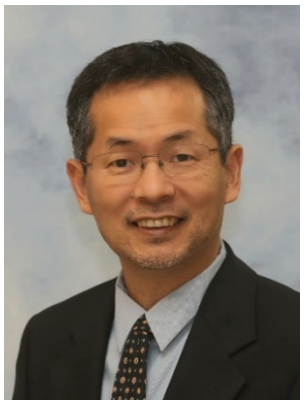

Xiaoning Ye, IEEE Fellow

Intel

Bo Pu

DeTooLIC Technology

Ling Zhang

Zhejiang University

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The TPC are led by the TPC Chairs including **Dr. Xiaoning Ye**, **Dr. Bo Pu,** and **Prof. Ling Zhang**. The Technical Committee members for the 2025 WAI are listed as below (sorted by last name).

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GENERAL INFORMATION

REGISTRATION

Registration link:

please register an account at http://www.wai-emc.com/wai2025/registration.

Each participant or each presenting author must pay a non-refundable pre-registration fee. Only pre-registered and paid submissions before 26 October, 2025 will be scheduled in the symposium program. Inclusion of the submissions in the final Technical Program (one-page abstracts only), and WAI Proceedings (one-page abstracts only) is guaranteed only after the pre-registration of the presenting author is completed.

Your pre-registration will be valid only provided the payment is received timely. The pre-registration deadline is 26 October, 2025. The on-site registration opportunity is for non-presenting authors only. The registration fee for your articles is non-refundable. The registration fee is the same for presenting authors and non-presenting authors.

Onsite Participants	Registration Fee
Student Full Price Ticket	RMB 1480 (USD 208)
Regular Full Price Ticket	RMB 2480 (USD 348)

CONFERENCE VENUE

HUALUXE® Ningbo Harbor City

The HUALUXE Hotel in Ningbo Port City is a new high-end five-star hotel brand under the InterContinental Hotels Group. Based on a globally renowned excellent management system, it is committed to providing you with a space that is close to nature and luxurious, bringing a new definition of Chinese hospitality to the Chinese people with "courtesy, respect, harmony, and expressiveness".

It is your ideal choice for business socializing and gathering with family and friends. The Huayi Hotel in Ningbo Port City understands the business and social needs of Chinese people. From relaxed meetings at the "Jumingyi" tea house, private banquets at the "Jushanyi" VIP world, to leisure and wellness at the Huayi Health Club, a series of public and private spaces fully meet the various business, social, and leisure entertainment needs of guests.

LOCATION MAP AROUND THE CONFERENCE VENUE

★HUALUXE® Ningbo Harbor City

Address: No. 1199 Changjiang Road, Beilun District, Ningbo City, Zhejiang Province

(+86 574 86799999)

Website: https://www.ihg.com.cn/hualuxe/hotels/cn/zh/ningbo/ngbul/hoteldetail#

REGISTRATION HOURS/FLOOR PLAN

Admission to all sessions and hosted functions requires the attendance identification. Please wear your name badge at all times.

Registration time

☐ November 4, Tuesday 14:00 - 19:00

☐ November 5, Wednesday 7:30 – 9:00

Registration Address

HUALUXE® Ningbo Harbor City

宁波港城华邑酒店

No. 1199 Changjiang Road, Beilun District, Ningbo City, Zhejiang Province

EXHIBITION HALL AND MEETING ROOMS

Opening Ceremony (开幕式及大会讲座)

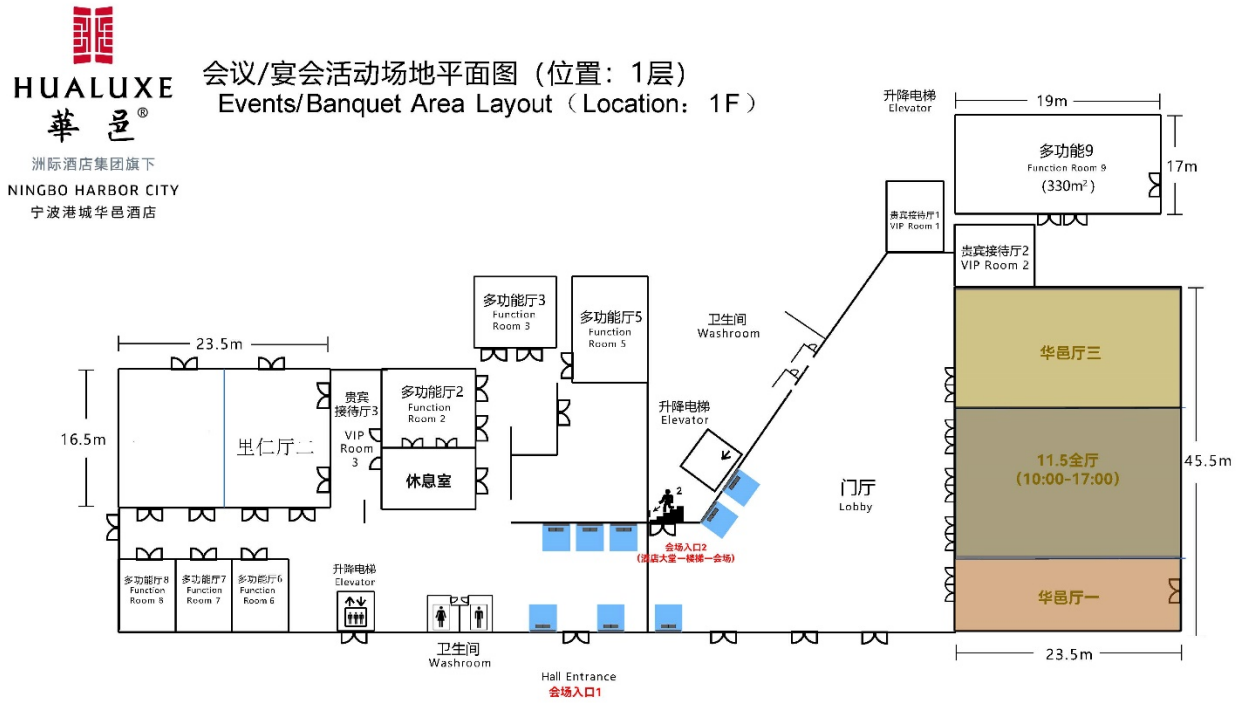
HUALUXE Hall @Level 1（1 楼华邑宴会厅）

Parallel Sessions (分会场)

Room 1: HUALUXE Hall 1 @Level 1（1 楼华邑厅一）

Room 2: HUALUXE Hall 3 @Level 1（1 楼华邑厅三）

Room 3: Liren Hall 2 @Level 1（1 楼里仁厅二）



PROGRAM OVERVIEW

Symposium Web: http://www.wai-emc.com/wai2025/

Symposium Hours

November 5, 2025, 8:30 – 17:30

November 6, 2025, 8:40 – 17:40

November 7, 2025, 8:40 – 11:40

November 5 – Wednesday

- ☐ Official Opening and Keynote Speeches
- ☐ Industry Plenary
- ☐ Technical Exhibition

November 6 – Thursday

- ☐ Oral Presentation
- ☐ Young Professional Session
- ☐ Technical Exhibition
- ☐ Banquet Dinner

November 7 – Friday

- ☐ IBIS Summit
- ☐ Oral Presentation
- ☐ Technical Exhibition

2025 International Workshop on Advanced Interconnects

November 5-7, 2025

Date	Time	Agenda
Nov. 5th	08:30-08:40	**Opening Ceremony**
	08:40-12:20	**Keynote Speeches**
	12:20-14:00	**Lunch**
	14:00-15:30	**Industry Plenary**
	15:30-15:50	**Tea Break**
	15:50-17:20	**Industry Plenary**
	17:30	**Dinner（Buffet）**

2025 International Workshop on Advanced Interconnects
November 5-7, 2025

Date	Time	HUALUXE Hall 1（华邑厅一）	HUALUXE Hall 3（华邑厅三）	Liren Hall 2 （里仁厅二）
Nov. 6th	8:40-10:00	*[SS1] Signal and Power Integrity for High-Speed Interconnect Design*	*[SS3] Advance in Electromagnetism Simulation and Analysis Method*	*Industry Plenary Talk (I-II)*
	10:00-10:20	**Tea Break**		
	10:20-11:00	*[SS1] Signal and Power Integrity for High-Speed Interconnect Design*	*[SS3] Advance in Electromagnetism Simulation and Analysis Method*	*Panel Discussion I* *Addressing the Ever-Growing Challenges in High-Speed Interconnect Designs in the AI Era: EDA Perspectives*
	11:00-12:00	*[SS1] Signal and Power Integrity for High-Speed Interconnect Design*	*[SS3] Advance in Electromagnetism Simulation and Analysis Method*	
	12:00-13:20	**Lunch & Rest**		*Young Professional Session (providing lunch)*
		HUALUXE Hall 1（华邑厅一）	**HUALUXE Hall 3（华邑厅三）**	**Liren Hall 2（里仁厅二）**
	13:20-14:00	*[SS2] Recent Advances in EMI/EMC Techniques*	*[SS5]* **Machine Learning Based EMC/SI/PI Design**	*Panel Discussion II* *Data Center High-Speed Interconnect in the AI Era: Part I - Innovations in Materials and Manufacturing*
	14:00-14:40	*[SS2] Recent Advances in EMI/EMC Techniques*	*[SS5]* **Machine Learning Based EMC/SI/PI Design**	
	14:40-15:20	*[SS2] Recent Advances in EMI/EMC Techniques*	*[SS5]* **Machine Learning Based EMC/SI/PI Design**	*Panel Discussion III* *Data Center High-Speed Interconnect in the AI Era: Part II - Architecturing the Interconnect for the Future*
	15:20-15:40	**Tea Break**		
	15:40-16:40	*[SS4] Power Integrity Design Techniques*	*[SS6] Antenna and Metasurface Design Techniques*	*Panel Discussion IV* *Trends in Smart Devices and Challenges Related to Electromagnetic Interference in the AI Era*
	16:40-17:40	*[SS4] Power Integrity Design Techniques*	*[SS6] Antenna and Metasurface Design Techniques*	
	18:30	**Banquet Dinner**		
Nov. 7th	**Time**	**HUALUXE Hall 1（华邑厅一）**	**HUALUXE Hall 3（华邑厅三）**	**Liren Hall 2 （里仁厅二）**
	8:40-9:40	*[SS7] Electromagnetic Compatibility of Integrated Circuits and Components*	*[SS8] Advanced Signal Integrity Modeling, Design, and Testing Techniques*	*IBIS Summit*
	9:40-10:00	**Tea Break**		
	10:00-11:40	*[SS7] Electromagnetic Compatibility of Integrated Circuits and Components*	*[SS8] Advanced Signal Integrity Modeling, Design, and Testing Techniques*	*IBIS Summit*
	END			

KEYNOTE SPEECHES I

TITLE	**High-Speed Interconnect in Data Centers**
TIME	8:40 – 9:20, November 5th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	Xiaoning Ye

ABSTRACT

The data center is undergoing a profound shift from CPU-centric design to accelerated computing and generative-AI–centric architectures. The fundamental unit of compute is no longer a single server but a distributed system at rack and cluster scale. Achieving performance now hinges on massive data parallelism—and the interconnect has become the first-order constraint as system scale and bandwidth rise.

This speech traces the evolution of high-speed interconnects in modern data centers and explains why signal integrity now drives the ecosystem. We will also show how hardware-architecture innovations can relieve interconnect bottlenecks and unlock scalable performance.

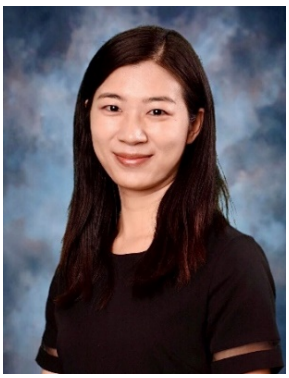
BIOGRAPHY

Dr. Xiaoning Ye is currently a Senior Principal Engineer at Data Center Group of Intel Corporation, specialized in high-speed interconnects. He received his Bachelor's and Master's degrees in electronics engineering from Tsinghua University, Beijing, China, in 1995 and 1997 respectively, and Ph.D. degree in electrical engineering from Missouri University of Science and Technology in 2000.

Dr. Ye published over 100 technical papers in IEEE and other technical journals and conferences, with over 3600 citations. He holds 20 patents and a few more applications in the areas of high-speed signaling. He also led the development of two industry standards on interconnect characterization: IEEE 370, and IPC test method 2.5.5.14. Dr. Ye is currently serving as Vice President of Technical Services for IEEE EMC Society. He was Chair of the IEEE EMC Society Technical Advisory Committee from 2017 to 2020, and has been an Associate Editor of IEEE Transactions on Electromagnetic Compatibility since 2016. Dr. Ye received Technical achievement award of IEEE EMC Society in 2015, and was elevated to IEEE fellow in 2021.

KEYNOTE SPEECHES II

TITLE	**Accelerating Innovation: AI-Driven Advances in Sigrity, Clarity, and Optimality**
TIME	9:20 – 10:00, November 5th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	Qin Liu



ABSTRACT

With the electronic systems being more complex, efficiency and accuracy requirement on design and simulation is becoming more and more demanding. At Cadence, we're meeting this challenge head-on by bringing AI and automation to every stage of design. Sigrity-APX, as an intelligent advanced IC Package Extractor, embeds machine learning model in many typical but challenging structures, such as vias, degassing hole planes, and traces with degassing hole planes. Clarity-PI is also launched as an AI accelerated Clarity extraction tool with faster, smarter and more stable solution, benefitting IC, interposer, and packaging extraction applications. Also, with new statistical functions and AI surrogate models, our advanced optimization engine allows user to explore the design space with higher efficiency. Furthermore, major break through is made in using generative AI beyond traditional optimization, we can now automate the entire workflow inside the design platform by creating new design from scratch, identifying critical regions, auto-cutting and extracting, and running targeted optimizations. AI algorithm, learning from Cadence's massive simulation datasets, predicts electromagnetic effects with high fidelity. This means fewer manual tweaks and more reliable results, accelerating the path to signoff.

BIOGRAPHY

Qin Liu is a Software Engineering Director in Sigrity R&D US Group at Cadence Design Systems, mainly focused on Clarity 3D full-wave electromagnetic software development. Dr. Liu has over 14 years' experience in developing advanced electromagnetic analysis and simulation methods. She received the B.Eng. degree in electronic engineering from the University of Science and Technology of China, Hefei, China, in 2011, and the Ph.D. degree in electrical and electronic engineering from The University of Hong Kong, Hong Kong, in 2015. From 2015 to 2018, she is a Post-Doctoral Fellow with The University of Hong Kong and a Postdoctoral Research Associate with the University of Illinois at Urbana Champaign. Since 2018, she has been working for Sigrity/Clarity R&D Group at Cadence Design System, San Jose, USA.

KEYNOTE SPEECHES III

TITLE	**High-Speed Interconnects in Semiconductor Systems: Where Physics Meets Performance**
TIME	10:20 – 11:00, November 5th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	En-xiao Liu

ABSTRACT

As semiconductor scaling is knocking on the door of the physical limits, interconnects open a new window into the spotlight of realizing system speed, bandwidth, energy, and reliability.

In this dense and deep connection era, multi-GHz signalling amplifies loss, crosstalk, and electrical and electromagnetic as well as multiphysics interactions across chip, package, and board hierarchies. Signal integrity, power integrity, and electromagnetic compatibility (SI/PI/EMC) can only be better achieved through multi-parameter and multi-objective early co-design and co-optimisation.

On one hand, advanced packaging, chiplets, and co-packaged optics create dense, multi-modal channels offering new hopes and new promises. On the other hand, AI and Machine learning (ML) are demanding even more from high-speed interconnects.

Can we leverage new physics, novel materials, heterogeneous architectures, AI/ML, and so on, to transform interconnects from passive links into active enablers of ultra-wide bandwidth, high-speed, energy-efficient, and robust systems?

BIOGRAPHY

En-Xiao Liu is currently Senior Principal Scientist and Deputy Department Director at A*STAR Institute of High Performance Computing. He is also an adjunct Associate Professor at the National University of Singapore. His research interests are in the areas of computational electromagnetics, high-speed electronics and packaging, electromagnetic compatibility (EMC), and AI/ML applications.

Dr. Liu received the team award of Singapore President's Technology Award (2019), ASEAN and IES Prestigious Engineering Achievement Award (2019), and the IEEE EMC Society Technical Achievement Award (2016). He was an IEEE EMC Society Distinguished Lecturer, the past Chair of the IEEE EMC Singapore Chapter, and TPC/General Chair for several international conferences. He is an Associate Editor of four IEEE journals (T-EMC, T-SPI, L-EMCPA, and T-CPMT). He co-edited the T-EMC (a) Special Section on Nature-Inspired Algorithms for EMC/SI/PI (2018) and (b) the Special Issue on AI/ML & Deep Learning for EMC (2024). He was a plenary speaker at the EMC Japan/APEMC Okinawa 2024 Symposium.

KEYNOTE SPEECHES IV

TITLE	**New Opportunity, New Journey**
TIME	11:00 – 11:40, November 5th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	Stanley Zheng

ABSTRACT

With the rapid development of digitization, intelligence, and the great prospect of semiconductor industry, we are standing at an unprecedented node in the window where there are constrains of supply chain and technology bifurcations, this presents both new opportunities and unprecedented challenges, requiring industry and academia to jointly explore technological breakthrough with STCO Collaborative Development

BIOGRAPHY

Stanley Zheng graduated from the Department of Computer Science at Fudan University and holds an MBA from Macau University of Science and Technology. He has served as Senior Engineer at Inventec, Engineering Manager at Phoenix Technologies, Technical Support Manager/Strategy Director at Intel, and Director of Semiconductor Industry Development at Huawei. His work experience spans OS development, BIOS/EFI development, chip technical support, marketing, ecosystem promotion, IP strategy, 7nm chip product development, and industry development. He is the only person in Intel China ever served as a global chip leader. He currently serves as the Director of External Cooperation Committee and Chief of Standards at EDA².

KEYNOTE SPEECHES V

TITLE	**Multiphysics EDA: Advanced Computing beyond Simulation**
TIME	11:40 – 12:20, November 5th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	Qiwei Zhan

ABSTRACT

When discussing multiphysics modeling, the finite element method is one of the most widely used algorithms. However, especially for complex systems, there remains a significant gap between real-world requirements and current simulation capabilities. This challenge arises mainly due to extreme problem scales, unavoidable uncertainties, and prolonged simulation times.

Moreover, with IC design having entered the post-Moore's Law era, 3D chip integration has emerged as one of the most promising technologies. Yet, an effective EDA tool that incorporates coupled electromagnetic, thermodynamic, and fluid effects is still lacking.

These challenges motivate us to develop multiphysics EDA software, by integrating recent advances in computational methods and going beyond conventional FEM simulation. To be more specific, this talk will present interdisciplinary efforts, toward the systematic integration of CAD (mesh generation), CAE (unified discontinuous Galerkin methods), and CAM (data learning), empowered by the high-performance computing technology.

BIOGRAPHY

Qiwei Zhan received the B.S. degree in geophysics from the University of Science and Technology of China, Hefei, China, in 2013, and the M.S. degree in civil and environmental engineering (minor) and the Ph.D. degree in electrical and computer engineering from Duke University, Durham, NC, USA, in 2016 and 2019, respectively. From June 2019 to August 2020, he was a Peter O'Donnell Jr. Postdoctoral Fellow with the Oden Institute for Computational Engineering and Sciences, The University of Texas at Austin, Austin, TX, USA. Since September 2020, he has been a Tenure-Track Professor and a Ph.D. Supervisor with the College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China. His research interests include multiphysics modeling, high-performance computing, uncertainty quantification, inverse problems, and scientific machine learning.

INDUSTRY PLENARY I

TITLE	**China's RISC-V High-Performance Computing: Exploration from Self-Developed IP to Ecosystem Construction**
TIME	14:00 – 14:30, November 5th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	Qingyuan Ren

ABSTRACT

This speech examines RISC-V's disruptive role in high-performance computing (HPC), highlighting global momentum and China's accelerated progress through strategic policy support. One of this evolution is RiVAI Technologies' Lingyu Processor—featuring a dual-core architecture, self-developed Core & NoC IP, and enterprise-grade RAS for data-center reliability. The speech further demonstrates a full-stack RISC-V HPC solution encompassing hardware co-developed with top OEMs and domestic software partners. Empowered by a robust ecosystem, RISC-V is advancing scenario-specific deployments (AI inference, industrial HPC) toward a multi-billion-dollar market, redefining next-generation computing infrastructure.

BIOGRAPHY

Mr. Ren Qingyuan graduated from Duke University and the University of Washington in the United States and previously held positions at leading industry companies such as Lenovo. In 2023, he joined RiVAI Technologies as Business Vice President, where he oversees the company's commercial and marketing operations.

INDUSTRY PLENARY II

TITLE	**Testing Solutions for Ultra-High-Speed Products ----- Signal Integrity Testing for Passive Components**
TIME	14:30 – 15:00, November 5th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	Xiangyang Ma

ABSTRACT

With the advent of generative AI, artificial intelligence has achieved leapfrog development in the 2020s, placing higher demands on hardware in terms of computing power, storage, and data transmission—requiring faster iteration, higher speeds, and quicker responses. In an increasingly demanding market, how can we grasp the right direction and solutions for product R&D and manufacturing to create better products? Share Dloorplf's solutions.

BIOGRAPHY

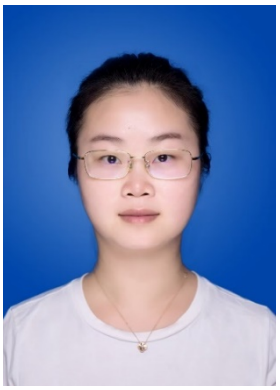
Industry-leading expert developers: Proficient in high-frequency and millimeter-wave communications, with 24 years of industry experience. Expertise in network analysis, S-parameters, DCA, RF SI, and related systems and development technologies.

•Possesses extensive project development management experience, having led full-cycle development and team management for 10G/40G Ethernet, 100G SR4/LR4, wireless modules, Apple millimeter-wave matrix, and 400G/800G optical transmission test systems. Expertise spans optical transmission, high-frequency transmission and integrity, and wireless signal system processing.

•Proficient in both software and hardware: Expertise in C/VB language interface systems, mastery of high-frequency PCB design and signal processing.

INDUSTRY PLENARY III

TITLE	**Development Status of InP and CMOS Heterogeneous Integration Technology**
TIME	15:00 – 15:30, November 6th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	Rong Chen



ABSTRACT:
InP and CMOS are two distinct semiconductor materials with its unique advantages and limitations. InP materials feature high electron mobility and high cutoff frequency, making them suitable for high-frequency and optoelectronic device fabrication. CMOS materials offer high electron mobility and high integration density, making them ideal for digital integrated circuits. To achieve frequencies of >100 GHz, the heterogeneous integration of InP and CMOS can offer superior performance and application value. However, there are several technical challenges in the integration process： particularly concerning material compatibility, device interoperability, and manufacturing processes. As a result, the heterogeneous integration of InP and CMOS has become a key area of research in recent years. This paper analyzes the development status of InP and CMOS heterogeneous integration technology, examines the main challenges currently faced by the technology, and explores future development directions, providing strong support for high-frequency (>100 GHz) wireless communications, radar imaging, and other high-performance applications.

BIOGRAPHY
Rong chen is an advanced packaging expert at CETC Chip Institute and Head of the Microsystem Integration Group at the National Laboratory of Integrated Circuits and Microsystems. She has led or participated in over ten national and ministerial-level key projects. Her current research is dedicated to 2.5D packaging and Chiplet technologies for high-speed, high-precision mixed-signal circuits, with over 10 publications and 3 patents.

INDUSTRY PLENARY IV

TITLE	**Research on Simulation and Testing of Signal Integrity and Power Integrity**
TIME	15:50 – 16:20, November 5th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	Jianguo Zhang

ABSTRACT
This article mainly introduces the work on SI fitting of encapsulated high-speed ABF materials and the simulation study on PI noise consistency. It focuses on how, during the material fitting process, the return loss SDD11 can be kept within an error of less than 1 dB, and how the PI noise error can be maintained within 5%.

BIOGRAPHY
Master's degree in Electromagnetic Field from University of Electronic Science and Technology of China.
Joined ZTE Microelectronics in 2021 as a Level 5 Technical Expert in the SIPI field, responsible for SIPI simulation technology and methodology for the packaging team, and serves as the head of the Chengdu Packaging Department.
Previously worked at several well-known companies in the industry, offers basic SI simulation courses.
Personal public account: <High-Speed Circuits and Signal Integrity>， @Half a RF Engineer

INDUSTRY PLENARY V

TITLE	**Speed Up 112/224G Design with Clarity 3D Solver and Optimality Explorer**
TIME	16:20 – 16:50, November 5th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	Kezhou Li

ABSTRACT:

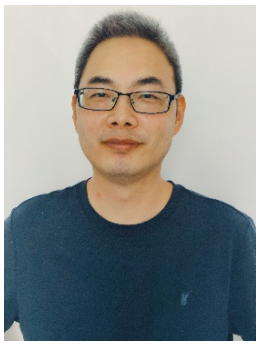
As cloud applications and large language models like GPT become increasingly widespread, network providers are compelled to upgrade transmission bandwidth, which requires advanced SerDes technology. The OIF organization initiated the CEI-224G project in 2020; if the 112G SerDes PAM4 scheme is adopted, the fundamental frequency reaches 56GHz, posing significant challenges for high-speed signal transmission across entire systems. Conventional design and simulation workflows often optimize individual components, but robust SerDes development at 112/224Gbps demands entire channel path analysis and system-level design optimization, accounting for all components' interactions. This presentation introduces how Cadence Clarity 3D Solver and Optimality Explorer efficiently enable global design and optimization for 112/224Gbps SerDes.

BIOGRAPHY

Kezhou Li is a seasoned expert in electromagnetic simulation with over 15 years of experience. As a Director in Cadence's System Design and Analysis (SDA) Group, Kezhou leads the Product Engineering and Verification Team in China. He has witnessed Cadence's remarkable growth in the system simulation domain and plays a key role in shaping the roadmap for flagship tools in electronic simulation.

INDUSTRY PLENARY VI

TITLE	**Evaluation and Solutions for Electrothermal and Mechanical Stress CHall enges in Large-Chip Applications**
TIME	16:50 – 17:20, November 5th
VENUE	HUALUXE Hall @Level 1（1 楼华邑宴会厅）
SPEAKER	Yi Chen



ABSTRACT

With increasing chip size and power consumption, the electrical, thermal, and mechanical stress issues in chip applications are becoming deeply intertwined. This article introduces evaluation methods and corresponding solutions to address these electro-thermal-stress challenges.

BIOGRAPHY

Earned a Master's degree from Harbin Institute of Technology. Joined ZTE Corporation in 2007 and possesses 20 years of experience in hardware development. Currently serving as the principal leader of the SI/PI team for wireless digital hardware and server products, with focused expertise in SerDes/DDR high-speed interface hardware design, evaluation, as well as SI/PI research related to chip packaging solutions and BBU/server architecture.

INDUSTRY PLENARY TALK I

TITLE	**Electromagnetic Compatibility (EMC) Simulation Applications in a Full-Vehicle Environment.**
TIME	8:40 – 9:10, November 6th
VENUE	Liren Hall 2 @Level 1（1 楼里仁厅二）
SPEAKER	Ming Zhou

ABSTRACT

Electromagnetic Compatibility (EMC) Simulation Applications in a Full-Vehicle Environment. Abstract: Full-vehicle EMC simulation faces significant challenges, including numerous EMI noise sources, complex noise propagation paths, difficulties in model simplification, and the inability to easily create simulation models from within components. CST Studio Suite has a wealth of application cases in full-vehicle EMC simulation, covering simulations for Conducted Emissions (CE), Radiated Emissions (RE), and Bulk Current Injection (BCI).

BIOGRAPHY

Zhou Ming earned his Master of Engineering degree from Harbin Institute of Technology. He has long specialized in electromagnetic field simulation technology research and possesses rich engineering application experience, providing CST simulation guidance and technical support to major clients in the high-tech and automotive industries.

INDUSTRY PLENARY TALK II

TITLE	**TBD**
TIME	9:10 – 9:40, November 6th
VENUE	Liren Hall 2 @Level 1（1 楼里仁厅二）
SPEAKER	TBD

ABSTRACT

TBD

BIOGRAPHY

TBD

Technical Sessions – Thursday, NOVEMBER 6, 2025

Room	*HUALUXE Hall 1*		*HUALUXE Hall 3*		*Liren Hall 2*
	SS1: Signal and Power Integrity for High-Speed Interconnect Design		**SS3: Advance in Electromagnetism Simulation and Analysis Method**		**Industry Plenary Talk**
SESSION CHAIR	***Francesco de Paulis,*** *University of L'Aquila, Italy*	***Seungyoung Ahn,*** *Korea Advanced Institute of Science and Technology, Korea (South)*	***Xiong Chen,*** *Xi'an Jiaotong University, China*	***Xiuqin Chu,*** *Xidian University, China*	***Ling Zhang,*** *Zhejiang University, China*
08:40-09:00	LPDDR SIPI Design Experience in Automotive Cockpit SoC and Microwave Nondestructive Evaluation Technique for Packaging Material (***Invited***) *(Chao Liu, Southeast University, China)*		Exploring Advanced Packaging in 2.5D/3D IC EDA: A Unified Platform for Backend Physical Design Simulation and Verification (***Invited***) *(Yi Zhao, Zhuhai Silicon Chip Technology Ltd., China)*		Electromagnetic Compatibility (EMC) Simulation Applications in a Full-Vehicle Environment **(*Invited*)** *（Ming ZHOU, CHINA SIMULIA Electromagnetics Industry Process Senior Consultant）*
09:00-09:20	Design and Analysis of Perforated Ground Plane for Mode Conversion Mitigation in High-Speed Differential Channel of Die-to-Die Interface *(Hyunwoo Kim, Korea Advanced Institute of Science and Technology University, Korea (South))*		Fast EM Algorithms for Interconnects in 2.5D/3D Integrated Circuits ***(Invited)*** *(Shunchuan Yang, Beihang University, China)*		***Industry Plenary Talk II***
09:20-09:40	Comparative Study of Delay Extraction Methods of Long SFP+ High Speed Cables for Signal Integrity Applications *(John Xiao, Keysight, China & Keysight (China), China)*		Physics-Constrained Differential Evolution for Continuous Decoupling Capacitor Placement and Orientation Optimization *(Li Jiang, Zhejiang University, China)*		
09:40-10:00	Modeling Capacitive-Loaded Unintentional Stubs in High-Speed Channels (*Nicolò Vicari, University of L'Aquila, Italy*)		Dielectric Reconfigurable S-band Planar Phase Shifter *(Yichen Liu, Xi'an Jiaotong University, China)*		***Panel Discussion***
10:00-10:20	Random Jitter Amplification Coefficient Calculation for NRZ PRBS Signal *(Tao Wei, Xidian University, China)*		Analysis of the Influence of Three - Proof Coating on the High - Speed Signal Transmission Performance of Embedded Computers *(Zichun Zhang, Xi'an Aeronautics Computing Technique Research Institute, China)*		
10:40-11:00	Comprehensive Measurement-to-Simulation Methodology for Better Gigabit Interconnect Evaluation and Exploration *(Tim Wang Lee, Keysight Technologies, USA)*		An Equation Based Solver for High-Speed Differential Pairs Affected by Fiber Weave Effect *(Kai Li, Cisco Systems, Inc., China)*		***Panel Discussion I*** Addressing the Ever-Growing Challenges in High-Speed Interconnect Designs in the AI Era: EDA Perspectives
11:00-11:20	Design Challenges and Optimization Strategies for High-Speed Connector Test Fixtures *(Lei Deng, LinkE Technologies, China)*		An Integrated Simulation Software for Component EMC Design and Analysis *(Jianhao Ge, Beihang University, China)*		
11:20-11:40	High-Order Markov Modeling of DFE Error Propagation Under Residual ISI Using SBR-Derived Transitions *(Yuhao Huang, Xidian University, China)*		Liquid Gated Network-Based Signal Integrity Analysis for High-Speed Links *(Yuxiang Tian, Zhejiang University, China)*		
11:40-12:00	Research on Physical Layer Signal Automated Testing Technology for Non-Standard Hardware Products *(Chuangye Guo, Avic Xi'an Aeronautics Computing Technique Research Institute, China)*		Addressing the Radio Frequency Interference Problem Through Characteristic Mode Analysis *(Xu Wang, Zhejiang University, China)*		

Room	*HUALUXE Hall 1*		*HUALUXE Hall 3*		*Liren Hall 2*
	SS2: Recent Advances in EMI/EMC		**SS5: AI/ML based EMC/SI/PI Design**		**Panel Discussion**
SESSION CHAIR	***Si-Ping Gao,*** *Nanjing University of Aeronautics and Astronautics, China*	***Huapeng Zhao,*** *University of Electronic Science and Technology of China, China*	***Dawei Wang,*** *Hangzhou Dianzi University, China*	***Xiaohe Chen,*** *China University of Petroleum, China*	***Bo Pu,*** *DeTooLIC Ltd. Technology, China*
13:20-13:40	Recent Progress of Fast Direct Partial Element Equivalent Circuit Method (***Invited***) *(Huapeng Zhao, University of Electronic Science and Technology of China, China)*		Application of Optimization Algorithms in Channel Signal Integrity Design *(Qihang Shang, DeTooLIC Ltd. Technology, China)*		***Panel Discussion II*** Data Center High-Speed Interconnect in the AI Era: Part I - Innovations in Materials and Manufacturing
13:40-14:00	Suppressing Evanescent Wave Coupling Using Anisotropic Metasurface in Small Cavity Circuit (***Invited***) *(Da Yi, Chongqing University, China)*		High-Speed Link Surrogate Modeling Based on Multimodal Machine Learning *(XiaoYang Wu, Hang Zhou Dian Zi University, China))*		
14: 00-14:20	Recent Advances in YIG-Based Frequency Selective Limiters *(Si-Ping Gao, Nanjing University of Aeronautics and Astronautics, China)*		An Efficient Thermal-Aware Placement Method for Chiplet-Oriented Integrated Microsystems *(Peng Zhang, Hangzhou Dianzi University, China)*		
14:20-14:40	A Reconfigurable Dual-Polarized Metasurface Capable of Switching Between Absorption and Transmission Modes *(Pei Zhang, Zhejiang University, China)*		Machine Learning-Assisted S-Parameter Frequency-Domain Extrapolation Method *(Fei Zhou, Hangzhou Dianzi University, China)*		***Panel Discussion III*** Data Center High-Speed Interconnect in the AI Era: Part II - Architecturing the Interconnect for the Future
14:40-15:00	Magnetic and Electric Shielding Effectiveness Measurement of System-in-Package *(Di Wang, Zhejiang University, China)*		DNN-Based Prediction of Frequency-Dependent RLGC Parameters for Transmission Lines *(Jiaqi He, Xidian University, China)*		
15:00-15:20	S-Band Tunable Impedance Matching Network with Varactor Diodes *(Zhou Han, Xi'an Jiaotong University, China)*		PCB Stack-Up Recognition Using LLMs *(Jie Li, Southwest University of Science and Technology, China)*		
	SS4: Power Integrity Design Techniques		**SS6: Antenna Design Techniques**		
SESSION CHAIR	***Jun Wang,*** *Xidian University, China*	***Xinglin Sun,*** *Zhejiang University, China*	***Guangxiao Luo,*** *North China Electric Power University (Baoding), China*	***Da Yi,*** Chongqing University, China	
15:40-16:00	A Hierarchical Optimization and Learning Framework for Broadband MLCC Equivalent-Circuit Modeling *(Yongjie Chen, Zhejiang University, China)*		An Efficient 2D/3D Mesh-Coupled Electro-Thermal Co-Simulation Method for Large-Scale Integrated Millimeter-Wave Phased Arrays *(Xinhong Xie, Donghai Laboratory, China)*		***Panel Discussion IV*** Trends in Smart Devices and Chall enges Related to Electromagnetic Interference in the AI Era
16:00-16:20	Calculation Method for Statistical Distribution of Power Supply Noise in Chip-Package-PCB Co-Design *(Yuhuan Luo, Xi'an University of Posts and Telecommunications, China)*		Computational Modeling of a Microstrip Antenna and Measurements with a Nano VNA *(Kenedy Marconi Geraldo Santos, IFBA, Brazil)*		
16:20-16:40	Multi-Objective Decap Optimization Based on Non-Dominated Sorting Genetic Algorithm *(Keyi Ding, Zhejiang University, China)*		CPW Antenna for Satellite Earth Mapping and Radiolocation Systems *(Marcelo B Perotoni, UFABC, Brazil)*		
16:40-17:00	Overestimation of Inductance in PDN Modeling: A Study on MLCC Models *(Cailiang Fu, Southwest University of Science and Technology, China)*		Dual Wideband Metasurface Based Linear to Circular Polarizer for Transmission Mode *(Fatima Ghulam, Zhejiang Normal University, China)*		
17:00-17:20	Attention-Guided Reinforcement-Genetic Optimizer: Fast PDN Impedance Prediction and Decoupling Capacitor Design for Power Integrity *(Qiyu Jiang, Beijing University of Posts and Telecommunications, China)*		Spiral Blade-Inspired Polarization-Insensitive X-Band FSS for EMI Shielding Applications *(Saad Hassan Kiani, Universiti Teknikal malaysia, Melaka, Malaysia)*		
17:20-17:40	Simulation and Test of 112Gbps SerDes Power Noise *(Lingyun Liu, SANECHIPS Technology CO. LTD, China)*		Calibration of Simple Transient Electric Field Probe and Circuit-Based Waveform Reconstruction *(Guangxiao Luo, North China Electric Power University (Baoding), China)*		

Technical Sessions – Friday, NOVEMBER 7, 2025

Rooms	*HUALUXE Hall 1*		*HUALUXE Hall 3*		*Liren Hall 2*
	SS7: Electromagnetic Compatibility of Integrated Circuits and Components		**SS8: Advanced SI Modeling, Design, and Testing Techniques**		**IBIS Summit**
SESSION CHAIR	***Fayu Wan,*** *Nanjing University of Information Science and Technology, China*	***Anfeng Huang,*** *DeTooLIC Ltd. Technology, China*	***Lei Deng,*** *LinkE Technologies, China*	***Si-Ping Gao,*** *Nanjing University of Aeronautics and Astronautics, China*	
08:40-09:00	From Standard Interpretation to Testing Practice: Exploring the Path to High-Quality CDM Testing (***Invited***) *(Bingsheng Gao, ESDEMC Technology LLC, China)*		A de-Embedding Method for High-Speed Single-Ended Signals with Three-Port Test Fixture *(Rui Miao, Xidian University, China)*		
09:00-09:20	Research on the Influence of Signal Integrity of the Test Board on the CAN Transceivers Electromagnetic Interference Test *(Qi Li, National New Energy Vehicles Technology Innovation Center & Automotive Chip Testing and Evaluation Key Laboratory State Administration for Market Regulation, China)*		A Novel Method for Calculating Crosstalk de-Embedding Transfer Function in High-Speed Link (*Rui Chen, Xidian University, China*)		
09:20-9:40	A Broadband Miniature TEM Cell for IC EMC Measurement over 8 GHz *(Chenghao Lan, Jimei University, China)*		Novel Methodology for Electrical Performance Characterization of High-Speed Raw Cables Under Thermal Stress *(Jimmy Hsu, Intel, Taiwan)*		
10:00-10:20	Comparative Study of BSS Algorithms for Noise Source Localization *(Hailing Zhao, Southwest University of Science and Technology, China)*		Delay Matters: Enhancing S-Parameter Macromodeling Accuracy *(Chenxi Liu, DeTooLIC Ltd. Technology, China)*		**IBIS Summit**
10:20-10:40	Exploration of the Relationship Between Copper Foil Microstructure and Etching Behavior on PCB Signal Integrity *(Changdong Gu, Zhejiang Huanergy, China)*		Connectors for 400 Gbps-per-Lane Links: Challenges and Design Directions *(Lei Deng, LinkE Technologies, China)*		
10:40-11:00	Charged Device Model Electrostatic Discharge Sensitivity Tester Based on 3D Vision *(Minfeng Xia, Nanjing University of Information Science and Technology, China)*		Twinax Cables at 448 Gb/s: Challenges and Solutions *(Lei Deng, LinkE Technologies, China)*		
11:00-11:20	Integrated Coaxial Resonator for Reconfigurable Passive Intermodulation Testing *(Min Liang, Xi'an Jiaotong University, China)*		2.4 GHz Wideband Tunable Impedance Matching Network *(Bin Han, Xi'an Jiaotong University, China)*		
11:20-11:40	Tunable Phase Shifter Using Monolithic Sliding Triple-Line Structure *(Yuhan Liu, Xi'an Jiaotong University, China)*		Implementation of an Adaptive DFE Algorithm *(Wenbo Zhang, Avic Xi'an Aeronautics Computing Technique Research Institute', China)*		
11:40-12:00	A Method for Generating Approximately Non-Diffracting Möbius Rings *(Yueyi Yuan, Harbin Institute of Technology, China)*		Research on GMSL Testing Technology in Multi-Physical Field Environments *(Yuxu Huo, Avic Xi'an Aeronautics Computing Technique Research Institute', China)*		

PANEL DISCUSSION I

TOPIC	**Addressing the Ever-Growing Challenges in High-Speed Interconnect Designs in the AI Era: EDA Perspectives**
TIME	10:20 – 12:00, November 6th
VENUE	**Liren Hall 2（里仁厅二）**
PANEL CHAIR	Bo Pu, TPC chair, International Workshop on Advanced Interconnects (WAI)
INVITED PANELIST	Stanley Zheng, Director of External Cooperation Committee and Chief of Standards, EDA² Michael Liu, Senior product director, Empyrean Technology Haisan Wang, AE Director, Cadence Kefei Zhang, Technical Marketing Director, Semitronix Yin Sun, Vice President of Product Engineering, DeTooLIC Technology Ming Zhou, SIMULIA Electromagnetics Industry Process Senior Consultant, Dassault Systemes Haidong Zhang, Leading EM and Thermal Product Director, NineCube Xiuguo Jiang, EDA SE&CSM Manager, Keysight

KEY TOPICS INCLUDE:

- Global and local Market Demands: EDA of high-speed and high bandwidth interconnects for Chiplet, data centers, AI systems, and supercomputing infrastructure.
- Innovative Solutions and Future Trends: Exploring cutting-edge solutions and technological advancements to meet the industry's demands.

We invite you to join this unique opportunity to connect with industry leaders and shape the future of EDA for high-speed and high bandwidth interconnect technologies.

BIO OF PANEL CHAIR

Bo Pu, TPC chair, International Workshop on Advanced Interconnects (WAI)

Dr. Bo Pu is the TPC chair of WAI. He was a Staff Engineer in charge of design methodology for AP, SerDes, HBM2/2E/3, DDR5 and GDDR6 from 14nm to 3nm as well as responsible for collaborating with Cadence and ANSYS in Samsung Semiconductor HQ, Korea. Then he joined Missouri University of Science and Technology, MO, USA as an assistant research professor. Currently He is the VP of DeTooLIC Technology. He published over 50 technical papers and holds 15 patents about high speed links and 2.5D/3D ICs.

He is the TPC chair and Member of the IEEE WAI, IEEE EMCS, IEEE APEMC, ISEMC and ACES. He was also awarded the 2014 URSI Young Scientists Award, 2022 APEMC Outstanding Young Scientists Award, and the 2020, 2021 Distinguish reviewer of IEEE Transactions on EMC, 2023 Outstanding Associate Editor of IEEE Access. Dr. Pu is a recipient of the Technical Achievement Award from IEEE EMC Society.

BIOS OF INVITED PANELIST

Stanley Zheng, Director of External Cooperation Committee and Chief of Standards, EDA²

Stanley Zheng graduated from the Department of Computer Science at Fudan University and holds an MBA from Macau University of Science and Technology. He has served as Senior Engineer at Inventec, Engineering Manager at Phoenix Technologies, Technical Support Manager/Strategy Director at Intel, and Director of Semiconductor Industry Development at Huawei. His work experience spans OS development, BIOS/EFI development, chip technical support, marketing, ecosystem promotion, IP strategy, 7nm chip product development, and industry development. He

is the only person in Intel China ever served as a global chip leader. He currently serves as the Director of External Cooperation Committee and Chief of Standards at EDA².

Michael Liu, Senior product director, Empyrean Technology

Michael Liu is the senior product director of Empyrean Technology. He has more than 10 years of experience in ASIC chip design, manufacturing, and packaging EDA software product development and management, focusing on the planning, development, and promotion of EDA products. He helps Empyrean build up a mature Analog/Mixed-Signal design flow, and expand it to the fields of other full custom design such as flat panel display, signal chain, memory, RF and optoelectronics. He is building a reliability design methodology for design-manufacturing collaboration and a PPAC-oriented design-manufacturing packaging collaborative design solution. The solutions are widely adopted by national and international leading design houses.

Haisan Wang, AE Director, Cadence

Haisan Wang is an AE director from Cadence Multi-Physics System Analysis (MSA) service AE team. He mainly focuses on performing high performance chip system design by co-design and co-simulation technology. Prior to joining Cadence, he worked at Sigrity and Huawei.

Kefei Zhang, Technical Marketing Director, Semitronix

Kefei Zhang has over 20 years of work experience in the field of chip design services and IP/EDA. Having worked in various positions such as design, product planning, and marketing promotion in multiple IPO companies.

He has successfully planned multiple video and IoT chips. He has rich experience in product management and technical marketing within the fields of chiplet, high- performance SoC, and IP.

Yin Sun, Vice President of Product Engineering, DeTooLIC Technology

Dr. Yin Sun heads the Product and Technology departments at Ningbo Detoolic Technology Co., Ltd. She holds a Ph.D. from Missouri University of Science and Technology, an M.S. from The Hong Kong University of Science and Technology, and a B.S. from Fudan University. Her research focuses on signal and power integrity in high-speed integrated circuit chips and packaging, as well as electromagnetic compatibility.

Ming Zhou, SIMULIA Electromagnetics Industry Process Senior Consultant, Dassault Systemes

Zhou Ming earned his Master of Engineering degree from Harbin Institute of Technology. He has long specialized in electromagnetic field simulation technology research and possesses rich engineering application experience, providing CST simulation guidance and technical support to major clients in the high-tech and automotive industries.

Haidong Zhang, Leading EM and Thermal Product Director, NineCube

Zhang Haidong is currently leading FEM Electromagnetic and Thermal Product line at NineCube. He has over 10 years of specialized experience in electromagnetic simulation tools. He obtained a master's degree from Shanghai Jiao Tong University in 2012.

Xiuguo Jiang, EDA SE&CSM Manager, Keysight

Xiuguo Jiang is the Great China EDA SE&CSM Manager at Keysight Technologies, where he focuses on Signal Integrity, Power Integrity, and EMC. He has more than 15 years of experience in Hardware and Signal integrity. Prior to joining Keysight Technologies, Xiuguo worked on system and component design. In recent years, he has been focused on the modeling of PCB, Package, and Components as well as some challenges of signal integrity and power integrity. He is the author of over 5 books on SI, PI, and EE. He operates WeChat Official Account <Signal Integrity> as a founder. The follower is more than 60k. He holds 1 Chinese patent. He published 4 papers.

PANEL DISCUSSION II

TOPIC	**Data Center High-Speed Interconnect in the AI Era: Part I - Innovations in Materials and Manufacturing**
TIME	13:20 – 14:20, November 6th
VENUE	**Liren Hall 2（里仁厅二）**
PANEL CHAIR	Harrison Xue， Senior SI Architect, Lenovo
INVITED PANELIST	Jiangqi He, President, NINGBO Everstrong Technology Co., Ltd. Loong Jin, Product Manager, LUXSHARE-TECH Technology Co., Ltd. Fazhi Liu, Huaqin Technology Co., Ltd. Jinshan Ma, Product Manager of AI&HPC Products, IEIT Systems Jeff Pan, President, Zhejiang Huanergy Co., Ltd. Xiangnan Sun, Senior Manager of Codesign & Product Operations, Starsmicrosystem Co., Ltd. Yanwu Wang, Vice President, DeTool Technology Co., Ltd. Kepeng Zhai, Senior Manager of R&D, Kinwong Electronics Co., Ltd.

BIO OF PANEL CHAIR

Harrison Xue, Senior SI Architect, Lenovo

Harrison Xue Fei is a senior SI architecture in Lenovo CSP. He was a Technical Lead in Intel. He works on signal integrity of high-speed interconnect in server, storage, data center systems and desktop laptop. He published 20+ technical papers in technical conference and at Intel. He received his bachelor and master's degrees in UESTC, Chengdu, China in 2002 and 2005 respectively.

BIOS OF INVITED PANELIST

Jiangqi He, President, NINGBO Everstrong Technology Co., Ltd.

Dr. Jiangqi was an intel Principal Engineer on advanced packaging, power integrity, power delivery and associated server hardware engineering. He was the founder and the director of hardware research lab and technical vice president for Huawei's North America research institute. From 2019 he started up NINGBO Everstrong technology which is focusing on advanced materials for advanced packaging and high-speed interconnect. Dr. He published more than 50 technical papers and owns more than 80 U.S. patents. His recent interest is new materials to meet AI needs.

Loong Jin, Product Manager, LUXSHARE-TECH Technology Co., Ltd.

Loong Jin has over 15 years of professional experience in the high-speed connector and cable assembly industry, having planned and led the development of multiple product lines including SSIO, HSIO, and BP. He also possesses extensive experience in the application and practice of interconnect solutions.

Fazhi Liu, Huaqin Technology Co., Ltd.
Fazhi Liu has over 10 years of experience architecting and de-risking high-speed digital systems for data-centric applications. Provides technical leadership across the entire product lifecycle, from initial system architecture and material selection to production bring-up and failure analysis. Focused on the design and validation of PCIe Gen5/6 and 112G/224G PAM4 SerDes channels, alongside robust Power Integrity implementation to ensure system-level performance.

Jinshan Ma, Product Manager of AI&HPC Products, IEIT Systems
Jinshan Ma, specializing in the server industry, leads upstream and downstream product planning and R&D, driving technology implementation and product iteration. Possesses extensive cross-domain technical expertise, having previously worked at companies such as Moore threads, Sugon, and Zhongsheng Hongxin. Responsible for core tasks including GPU chip product planning, supercomputer system architecture design, and CPU chip system platform design, with comprehensive technical vision and practical capabilities spanning from chips and servers to supercomputing systems.

Jeff Pan, President, Zhejiang Huanergy Co.,Ltd.
Jeff Pan serves as the President of Zhejiang Huanergy Co., Ltd., which was founded in 2017 and the company specializes in high-end copper foil research and production in the electronics and lithium-ion battery industries. Jeff holds an MBA degree from the Fuqua School of Business, Duke University.

Xiangnan Sun, Senior Manager of Codesign & Product Operations, Starsmicrosystem Co., Ltd.
Xiangnan Sun is responsible for the packaging R & D and mass production operation of all the company's products. In the R&D part, he collaborates with the design team and is mainly in charge of the packaging and system SI of all the company's products, including package design, package and system SIPI simulation, thermal simulation, stress simulation, and package engineering. He is also responsible for the introduction of the company's chip packaging from NPI to mass production. In the operation part, he is mainly responsible for the mass - production shipment of all the company's products, production planning, production management, account reconciliation, and ERP system maintenance.

Yanwu Wang, Vice President, DeTool Technology Co.,Ltd.
Yanwu Wang focuses on EDA solutions for signal and power integrity design, optimization, and system solutions. He has over 20 years of experience in high-speed SerDes and DDR design for computer and server products. Before joining Detool, he was responsible for high-speed system design and product development at multiple companies.

Kepeng Zhai, Senior Manager of R&D, Kinwong Electronics Co., Ltd.
Graduated from Guilin University of Electronic Technology with a Bachelor's degree in Communication Engineering in 2015. Previously worked at a leading communication design company, responsible for the design and simulation of RF circuits and antennas for consumer electronic products. He joined in Kinwong in 2020 and be employed in a Senior Manager of R&D. Responsible for electromagnetic field analysis and design optimization of high-frequency and high-speed PCBs. Main research areas including high-speed interconnection modeling, simulation and measurement. This includes PCB material selection, stack-up design, material parameter extraction and design simulation verification.

PANEL DISCUSSION III

TOPIC	**Data Center High-Speed Interconnect in the AI Era: Part II - Architecturing the Interconnect for the Future**
TIME	14:20 – 15:20, November 6th
VENUE	**Liren Hall 2（里仁厅二）**
PANEL CHAIR	Harrison Xue， Senior SI Architect, Lenovo
INVITED PANELIST	Lei Deng, General Manager, Zhuhai LinkE Technology Co., Ltd. Jiangqi He, President, NINGBO Everstrong Technology Co., Ltd. Loong Jin, Product Manager, LUXSHARE-TECH Technology Co., Ltd. Fazhi Liu, Huaqin Technology Co., Ltd. Jinshan Ma, Product Manager of AI&HPC Products, IEIT Systems Anbing Sun, Senior Hardware System Engineer, Ruijie Networks. Xiangnan Sun, Senior Manager of Codesign & Product Operations, Starsmicrosystem Co., Ltd. Yanwu Wang, Vice President, DeTool Technology Co., Ltd. Kepeng Zhai, Senior Manager of R&D, Kinwong Electronics Co., Ltd.

BIO OF PANEL CHAIR

Harrison Xue, Senior SI Architect, Lenovo
Harrison Xue Fei is a senior SI architecture in Lenovo CSP. He was a Technical Lead in Intel. He works on signal integrity of high-speed interconnect in server, storage, data center systems and desktop laptop. He published 20+ technical papers in technical conference and at Intel. He received his bachelor and master's degrees in UESTC, Chengdu, China in 2002 and 2005 respectively.

BIOS OF INVITED PANELIST

Lei Deng, General Manager, Zhuhai LinkE Technology Co., Ltd.
Deng Lei has over 15 years of R&D experience in high-speed interconnects, antenna technology and high-performance RF system design. Currently, he is leading the team to develop cutting-edge solutions for next-generation connectivity. He holds a bachelor's and master's degree from Huazhong University of Science and Technology.

Jiangqi He, President, NINGBO Everstrong Technology Co., Ltd.
Dr. Jiangqi was an intel Principal Engineer on advanced packaging, power integrity, power delivery and associated server hardware engineering. He was the founder and the director of hardware research lab and technical vice president for Huawei's North America research institute. From 2019 he started up NINGBO Everstrong technology which is focusing on advanced materials for advanced packaging and high-speed interconnect. Dr. He published more than 50 technical papers and owns more than 80 U.S. patents. His recent interest is new materials to meet AI needs.

Loong Jin, Product Manager, LUXSHARE-TECH Technology Co., Ltd.
Loong Jin has over 15 years of professional experience in the high-speed connector and cable assembly industry, having planned and led the development of multiple product lines including SSIO, HSIO, and BP. He also possesses extensive experience in the application and practice of interconnect solutions.

Fazhi Liu, Huaqin Technology Co., Ltd.
Fazhi Liu has over 10 years of experience architecting and de-risking high-speed digital systems for data-centric applications. Provides technical leadership across the entire product lifecycle, from initial system architecture and material selection to production bring-up and failure analysis. Focused on the design and validation of PCIe Gen5/6 and 112G/224G PAM4 SerDes channels, alongside robust Power Integrity implementation to ensure system-level performance.

Jinshan Ma, Product Manager of AI&HPC Products, IEIT Systems
Jinshan Ma, specializing in the server industry, leads upstream and downstream product planning and R&D, driving technology implementation and product iteration. Possesses extensive cross-domain technical expertise, having previously worked at companies such as Moore threads, Sugon, and Zhongsheng Hongxin. Responsible for core tasks including GPU chip product planning, supercomputer system architecture design, and CPU chip system platform design, with comprehensive technical vision and practical capabilities spanning from chips and servers to supercomputing systems.

Anbing Sun, Senior Hardware System Engineer, Ruijie Networks.
Sun Anbing has more than 15 years of experience in PCB/SI and is currently focused on the hardware system architecture design and new technology research of the next-generation data center switche

Xiangnan Sun, Senior Manager of Codesign & Product Operations, Starsmicrosystem Co., Ltd.
Xiangnan Sun is responsible for the packaging R & D and mass production operation of all the company's products. In the R&D part, he collaborates with the design team and is mainly in charge of the packaging and system SI of all the company's products, including package design, package and system SIPI simulation, thermal simulation, stress simulation, and package engineering. He is also responsible for the introduction of the company's chip packaging from NPI to mass production. In the operation part, he is mainly responsible for the mass - production shipment of all the company's products, production planning, production management, account reconciliation, and ERP system maintenance.

Yanwu Wang, Vice President, DeTool Technology Co.,Ltd.
Yanwu Wang focuses on EDA solutions for signal and power integrity design, optimization, and system solutions. He has over 20 years of experience in high-speed SerDes and DDR design for computer and server products. Before joining Detool, he was responsible for high-speed system design and product development at multiple companies.

Kepeng Zhai, Senior Manager of R&D, Kinwong Electronics Co., Ltd.
Graduated from Guilin University of Electronic Technology with a Bachelor's degree in Communication Engineering in 2015. Previously worked at a leading communication design company, responsible for the design and simulation of RF circuits and antennas for consumer electronic products. He joined in Kinwong in 2020 and be employed in a Senior Manager of R&D. Responsible for electromagnetic field analysis and design optimization of high-frequency and high-speed PCBs. Main research areas including high-speed interconnection modeling, simulation and measurement. This includes PCB material selection, stack-up design, material parameter extraction and design simulation verification.

PANEL DISCUSSION IV

TOPIC	**Trends in Smart Devices and Challenges Related to Electromagnetic Interference in the AI Era**
TIME	15:40 – 16:40, November 6th
VENUE	**Liren Hall 2（里仁厅二）**
PANEL CHAIR	Anfeng Huang, DeTooLIC Technology
INVITED PANELIST	Yiqiang Zhang, Vivo software Technology co., Ltd.; Kaixiang Zhu, Honor; Kaiming Ding, Huaqin; Wenju Sheng, Huawei Device; Chengming Wang, Xiaomi;

BIO OF PANEL CHAIR

Anfeng Huang, Director, DeTooLIC Technology

Anfeng Huang (Member, IEEE) received the B.E. and M.S. degrees in electrical engineering from Xidian University, Shaanxi, China, in 2014 and 2017, respectively, and the Ph.D. degree in electrical engineering from the Missouri University of Science and Technology, Rolla, MO, USA, in 2022. He is currently with Detooltech, Ningbo, China. His current research interests include EMI in power electronics, magnetic material characterization, and advanced measurement techniques.

BIOS OF INVITED PANELIST

Yiqiang Zhang, Vivo software Technology co., Ltd.

Over 20+ EMC design experience in network equipment and mobile terminals

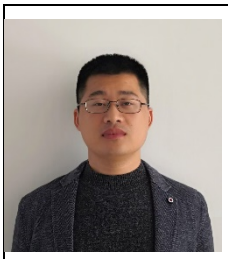
- vivo software Technology co., Ltd., EMC expert, started 2019
- TD Tech Communications co.,Ltd., EMC expert 2016-2019
- Nokia China, EMC expert, 2011-2015
- H3C, EMC design, 2005-2011

Kaixiang Zhu, Honor

Kaixiang Zhu received the B.S. degree and the Ph.D. degree from Beihang University, Beijing China, in 2013 and 2019. He is currently a Senior Engineer with Honor Device, working towards RF interference, susceptibility of multimedia module and other EMI problems in terminal products.

Kaiming Ding, Huaqin

Kaiming Ding is currently employed at Huaqin Technology Co., Ltd. as a Senior Advanced Engineer, with over 10 years of experience in EMC engineering projects. He is responsible for technical pre-research in the EMC direction at the Group Technology Center and has recently focused on the research and resolution of radio frequency interference, immunity, and nonlinear issues in the consumer electronics field.



Wenju Sheng, Huawei Device

Sheng Wenju, a graduate of Wuhan Institute of Technology, is the Director of the High-Frequency & High-Speed Capability Center and the Chief SI & PI Expert in the Terminal Interconnection Department at Huawei Device Co., Ltd. He is also recognized as a Level 7 Expert in Device Board-Level Hardware and Process. He specializes in Signal Integrity (SI) and Power Integrity (PI) engineering for mobile phones, tablets, and PCs in challenging scenarios characterized by high density, high bandwidth, strong interference, and low power consumption.

Chengming Wang, Xiaomi

Chengming Wang received his B.S. (2018) and M.S. (2021) degrees in Information Science and Electronic Engineering from Zhejiang University. He is currently a Senior Engineer at the Simulation Department of Xiaomi Corporation, where his work focuses on solving electromagnetic compatibility (EMC) challenges in mobile devices. His key responsibilities include the simulation and optimization of EMC performance for smartphones.

HOW TO GET TO THE HUALUXE® NINGBO HARBOR CITY

Taking the Airplane

Ningbo Lishe International Airport →HUALUXE® Ningbo Harbor City

→ Enter Lishe International Airport Station (toward Honglian).

→ Transfer at Gulou Station to Metro Line 1 (toward Xiapu)

→ Get off at Changjiang Road Station (Exit A1).

Taking the (High-speed)Train

Ningbo Station→HUALUXE® Ningbo Harbor City

→ Enter Ningbo Railway Station Metro (toward Honglian).

→ Transfer at Gulou Station to Metro Line 1 (toward Xiapu).

→ Get off at Changjiang Road Station (Exit A1).

→ Walk 436 meters to reach HUALUXE Ningbo Harbor City.

Driving by Yourself

Please search for "HUALUXE Ningbo Harbor City" in GPS. The navigation will plan your traffic route according to your current position.

Parking: HUALUXE Ningbo Harbor City

ACCOMMODATION

Special rates have been negotiated for the 2025 WAI in Ningbo attendees at HUALUXE Ningbo Harbor City.

If you need to book a room, please contact the hotel before November 1, 2025, quoting the name of the conference to make a reservation at the special rate.

Hotel Name：

HUALUXE Ningbo Harbor City
宁波港城华邑酒店

Hotel Address：
No. 1199 Changjiang Road, Beilun District, Ningbo City, Zhejiang Province
宁波市北仑区长江路 1199 号

Hotel Phone Number：
+86 574-86799999

Recommendations for other hotels:

Hotel Name：

Hanting Hotel (Ningbo Beilun Changjiang Road Subway Station Branch)

Hotel Phone Number：
+0574-26881666

The venue can be reached from the hotel in 8 minutes on foot (599 meters).

Hotel Name：

Ningbo Meike City Hotel

Hotel Phone Number：
+ 0574-86863066

The venue can be reached from the hotel in 6 minutes on foot (445 meters).

Hotel Name：

Yaduo Hotel, Beilun Youth Sports Center, Ningbo

Hotel Phone Number：
+86 574-27629888
The venue can be reached from the hotel in 8 minutes by car (1.2 km).

ABOUT NINGBO

Ningbo, also known as Yong, is located halfway down the coastline of the Chinese mainland and to the south of the Yangtze River Delta. It is bordered by the natural bulwark of the Zhoushan Archipelago to the east, the city of Shaoxing to the west, the city of Shanghai to the north across the Hangzhou Bay, and the city of Taizhou and Sanmen Bay to the south.

The city's history can be traced back to the Hemudu Culture that originated 7,000 years ago. In the Xia and Shang Dynasties about 4,000 years ago, Ningbo was known as Yin. Later, in the Spring and Autumn Period (770-476 BC), it became part of the State of Yue. In the Qin Dynasty (221-206 BC), it encompassed Yin, Mao and Gouzhang, three areas under the Kuaiji Shire. In the Tang Dynasty (618-907 AD), it was named Mingzhou. In 821 AD, the local authority moved towards the junction of three local rivers and built city walls, marking the establishment of today's city. In 1381 AD, the city acquired its current name of Ningbo, or, literally, Calm Waves.