WAI 2024 Ningbo, China November 6 – 8, 2024

2024 IEEE International Workshop on Advanced Interconnects
Ningbo, China

WAI 2024

November 6 – 8, 2024

Final Program

（浙江省）全省电磁智能感控与先进电子集成重点实验室

ORGANIZERS AND TECHNICAL SPONSORS

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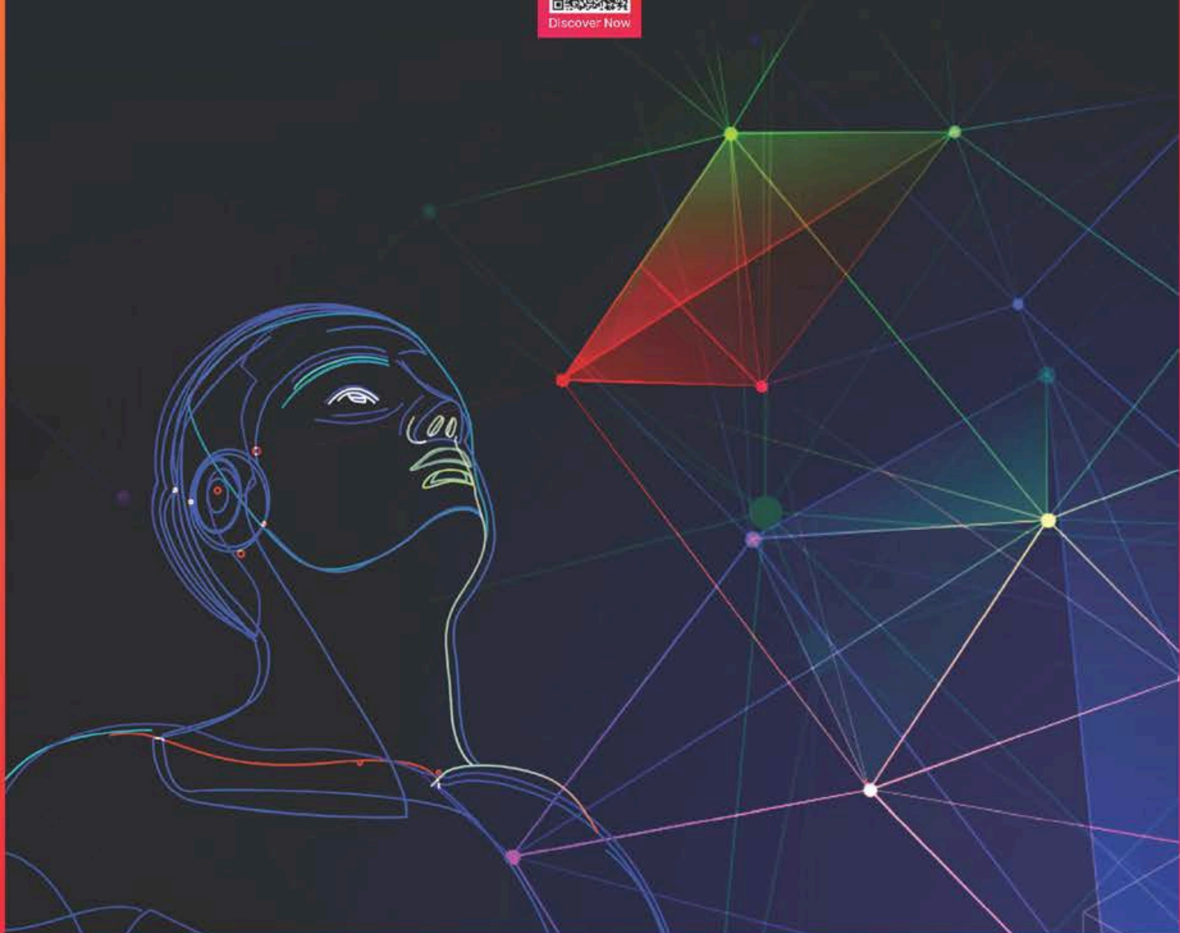

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产业领域：数据中心、电磁屏蔽机房、硬件研发、软件开发、涉密会议室

浙江绿色理想科技有限公司成立于1998年，专业从事数据中心的咨询、设计、建设、运维、分析等技术服务，多年来公司秉承“专业、诚信、创新、合作”的企业核心价值观，为用户提供专业的产品及整体解决方案。

在行业耕耘20多年，我司以数据中心建设及运维服务为业务核心，辐射咨询服务、软件开发、电磁产品研发等业务内容。结合多年的工程实施及运维管理经验，打造“ Green Ideal ”品牌，推出了数据中心统一运营平台(DCUMP)、电磁屏蔽、一体柜和多联柜等自主研发产品。

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INVITATION FROM THE GENERAL CHAIR

Dear Colleagues and Friends,

On behalf of the 2024 WAI Steering Committee, we are privileged and honored to invite you, your colleagues and families to join us for the flagship event of IEEE International Workshop on Advanced Interconnects (WAI) from Wednesday, Nov. 6th to Friday, Nov. 8th in Ningbo, China.

The IEEE International Workshop on Advanced Interconnects is a newly lauched IEEE event. The scope of this workshop includes, but is not limited to signal integrity and power integrity of an electronic system and its components including advanced interconnects, integrated circuits, IC packages, printed circuit boards, cables, connectors, as well as other relevant electronic and microelectronic components, and signal integrity/ power integrity co-design.

WAI will offer a rich scientific program of highest quality with keynote speakers, invited speakers and provide a broad forum of exchange for both academia and industry. The Workshop will cover the entire scope of interconnects SI/PI, multiphyics, electromagnetic compatibility and extend to the emerging technologies associated with interconnects such as artificial intelligence for interconnects and EMC/SI/PI design methodologies.

The IEEE EMC Society is the primary co-sponsor of this event, in collaboration with DeToolIC, Zhejiang University, Ningbo University, Southwest University of Science and Technology.

So come and join us in Ningbo in November of 2024 for an outstanding scientific/technical event and an unforgettable experience for you and your family.

WAI 2024 General Chairs

Jun Fan, IEEE Fellow

Qiushi Professor, Zhejiang University

Er-Ping Li, IEEE Fellow

Qiushi Chair Professor, Zhejiang University

CHAIRS FOR TECHNICAL PROGRAM COMMITTEE

Dear Colleagues and Friends,

Welcome to Ningbo!

On behalf of the Technical Program Committee, we are pleased to extend our warmest welcome to the 2024 IEEE International Workshop on Advanced Interconnects. This event provides an exciting opportunity to connect with colleagues, share insights, exchange ideas, and learn from leading experts and innovators.

Thanks to the diligent efforts of our organizing committees, we have assembled an engaging two-and-a-half-day program that includes:

- 4 keynote speeches from distinguished guests in industry and academia
- 7 industry plenary talks delivered by top experts in the field
- Around 60 organized oral presentations and 40 submitted abstracts in the poster format on cutting-edge advancements in advanced interconnect technologies
- 2 panel discussions addressing the latest design and development challenges in EDA and Solutions and Trends of High-Speed Cables and Connectors

We hope this extensive program offers valuable learning and networking opportunities for everyone. We look forward to meeting you in Ningbo!

Chairs of the Technical Program Committee

Xiaoning Ye, IEEE Fellow

Intel

Bo Pu

DeTooLIC Technology

Ling Zhang

Zhejiang University

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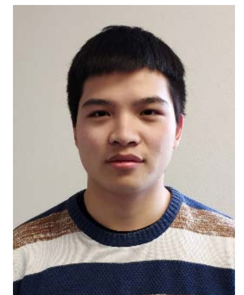

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Haiqing Zhang, DeTooLIC Technology, China

TECHNICAL PROGRAM COMMITTEES

The TPC are led by the TPC Chairs including **Dr. Xiaoning Ye**, **Dr. Bo Pu,** and **Prof. Ling Zhang**. The Technical Committee members for the 2024 WAI are listed as below (sorted by last name).

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Yuyu Zhu
Southwest University of Science and Technology, China

Cheng Zhuo
Zhejiang University, China

GENERAL INFORMATION

REGISTRATION

Registration link:

please register an account at http://www.wai-emc.com/wai2024/user/register.

Each participant or each presenting author must pay a non-refundable pre-registration fee and is limited to presenting no more than three papers in oral and poster sessions. Only pre-registered and paid submissions before 30 October, 2024 will be scheduled in the symposium program. Inclusion of the submissions in the final Technical Program (one-page abstracts only), and WAI Proceedings (one-page abstracts only) is guaranteed only after the pre-registration of the presenting author is completed. Your pre-registration will be valid only provided the payment is received timely.

Your pre-registration will be valid only provided the payment is received timely. The pre-registration deadline is 30 October, 2024. The on-site registration opportunity is for non-presenting authors only. The registration fee for your articles is non-refundable. The registration fee is the same for presenting authors and non-presenting authors.

Registration Fee	Onsite Participants
Student Fee	USD 180 / RMB 1260
Regular Registration Fee	USD 300 / RMB 2100

CONFERENCE VENUE

InterContinental Ningbo

The InterContinental Ningbo (Ningbo Zhouji Jiudian) is a 5-star hotel located in the National Hi Tech Development Industrial Zone within easy reach of the Yongxin River and the International Conference and Exhibition Center.

Diners can enjoy Western and local favorites throughout the day in the all-day dining restaurant, Elements. Cantonese, Ningbo and spicy Sichuan dishes are served at Lu Yuan, the on-site Chinese restaurant. The spacious lobby lounge provides a place to relax and enjoy a drink, whether taking-in an informal business meeting or winding down from a busy workday.

LOCATION MAP AROUND THE CONFERENCE VENUE

★ InterContinental Ningbo

Business zone: Jiangdong Business District (江东商业区)

Address: No.777 Xinhui Road, Yinzhou District, Ningbo, Zhejiang

(+86 574 89077777)

Website: http://ningbo.ihghotels.cn

REGISTRATION HOURS/FLOOR PLAN

Admission to all sessions and hosted functions requires the attendance identification. Please wear your name badge at all times.

Registration time

- ☐ November 5, Tuesday 14:00 - 18:00
- ☐ November 6, Wednesday 8:30 - 18:00

Registration Address

InterContinental Ningbo

777 Xinhui Road, National High-tech Zone, Ningbo City, Zhejiang Province

EXHIBITION HALL AND MEETING ROOMS

Opening Ceremony (开幕式及大会讲座)	Pacific Hall @Level 1（1 楼太平洋宴会厅）
Parallel Sessions (分会场)	Room 1: JiangNan Function Room @Level 2（2 楼江南厅） Room 2: YuanShi Function Room @Level 2（2 楼院士厅） Room 3: JuXian Function Room @Level 2（2 楼聚贤厅） Room 4: XinHui Function Room @Level 2（2 楼新晖厅）

太平洋宴会厅平面图（酒店1层）

Floor plan of banquet hall (1F)

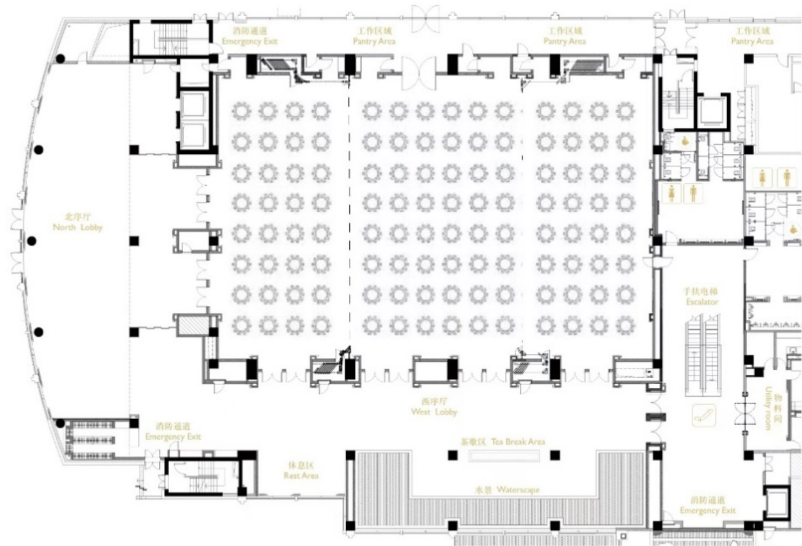
标识图例 Conventional signs

男洗手间 Men's room

女洗手间 Women's room

残疾人洗手间 Disabled restroom

手扶电梯 Escalator



宴会厅平面图（酒店2层）

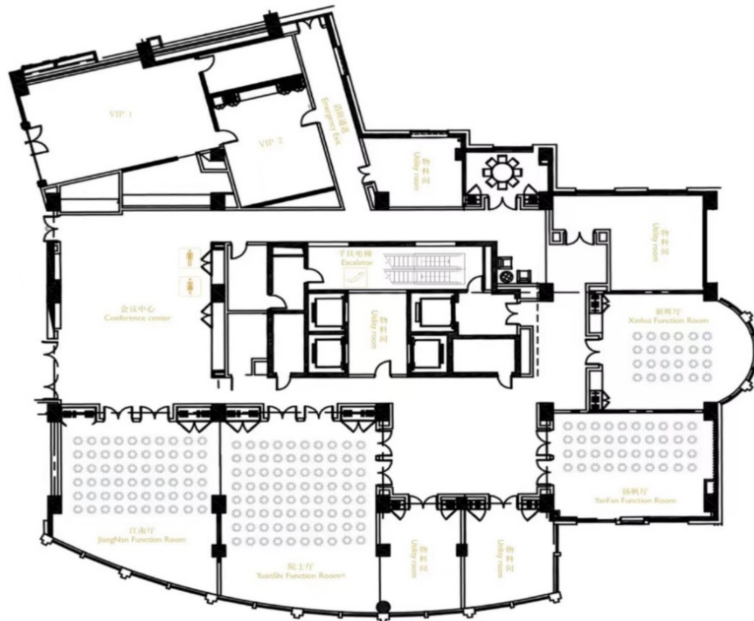
Floor plan of banquet hall (2F)

标识图例 Conventional signs

男洗手间 Men's room

女洗手间 Women's room

手扶电梯 Escalator



INSTRUCTIONS TO POSTER PRESENTERS

Poster Presentation

Poster sessions will be held at **Room 4** (XinHui Function Room @Level 2).
Please register at the Registration Desk before proceeding to locate your assigned poster board. To locate your assigned poster board, look for the board marked with your Paper ID.

Set-up Your Poster

- ☐ The WAI Organizing Committee Will Set-up Your Poster.
- ☐ Presenters are required to be at their posters during their scheduled Open forum session.

Remove Your Poster

Posters must be removed after the respective Open Forum sessions within half an hour.
Posters remaining after these times will be removed. WAI organizer will not be responsible for posters and materials left on poster boards after the stated hours.

Information Desk

Staff at the Information Desk will be available to assist you with location and other on-site needs. Tapes and scissors will be available for your use. If you have special needs for your poster presentation, please bring those supplies with you to the meeting.

PROGRAM OVERVIEW

Symposium Web: http://www.wai-emc.com/wai2024/

Symposium Hours

November 6, 2024, 8:30 – 17:00

November 7, 2024, 8:40 – 17:20

November 8, 2024, 8:30 – 11:40

November 6 – Wednesday

- ☐ Official Opening and Keynote Speeches
- ☐ Industry Plenary
- ☐ Technical Exhibition

November 7 – Thursday

- ☐ Technical Sessions
- ☐ Technical Exhibition

November 8 – Friday

- ☐ Technical Sessions
- ☐ Technical Exhibition

2024 IEEE International Workshop on Advanced Interconnects
November 6-8, 2024

Date	Time	Agenda
Nov. 6th	08:30-09:00	**Opening Ceremony**
	09:00-12:00	**Keynote Speeches**
	12:00-13:40	**Lunch**
	13:40-15:30	**Industry Plenary**
	15:30-15:50	**Tea Break**
	15:50-16:50	**Industry Plenary**
	18:30	**Banquet Dinner**

2024 IEEE International Workshop on Advanced Interconnects
November 6-8, 2024

Date	Time	Room #1 JiangNan Function Room(江南厅)	Room #2 YuanShi Function Room(院士厅)	Room #3 JuXian Function Room(聚贤厅)	Room #4 XinHui Function Room(新晖厅)
Nov. 7th	8:40-10:40	*SS1: Advanced SI Modeling, Design, and Testing Technologies*	*SS2: Advanced PI and Multiphysics Modeling, Design, and Testing Technologies*	*SS3: ESD Techniques for Integrated Circuits and Electronic Systems*	*Abstract Session (Poster Discussion)*
	10:40-11:00	**Tea Break**			
	11:00-12:00	*SS1: Advanced SI Modeling, Design, and Testing Technologies*	*Panel Discussion I (EDA for High Speed and High Bandwidth Interconnects)*	*SS3: ESD Techniques for Integrated Circuits and Electronic Systems*	
	12:00-13:30	**Lunch & Rest**			
		Room #1 JiangNan Function Room(江南厅)	**Room #2 YuanShi Function Room(院士厅)**	**Room #3 JuXian Function Room(聚贤厅)**	**Room #4 XinHui Function Room(新晖厅)**
	13:30-16:00	*SS4: EMC Techniques for Integrated Circuits*	*SS5: Advanced EMI Modelling and Measurement Technologies*	*SS6: Signal/Power Integrity and Multiphysics Analysis for Chiplets*	*Award Ceremony*
	16:00-16:20	**Tea Break**			
	16:20-17:20	*SS4: EMC Techniques for Integrated Circuits*	*SS5: Advanced EMI Modelling and Measurement Technologies*	*SS6: Signal/Power Integrity and Multiphysics Analysis for Chiplets*	*Panel Discussion II (Solutions and Trends of High-Speed Cables and Connectors)*
Nov. 8th	**Time**	**Room #1 JiangNan Function Room(江南厅)**	**Room #2 YuanShi Function Room(院士厅)**	**Room #3 JuXian Function Room(聚贤厅)**	
	8:30-10:30	*SS7: AI Assisted EMC/SI/PI Technologies*	*SS8: Electromagnetic Modeling, Design, and Measurement of Circuits, Devices, and Metamaterials*	*SS9: ESD/EMI Techniques for Electronic Systems*	
	10:30-10:40	**Tea Break**			
	10:40-11:40	*SS7: AI Assisted EMC/SI/PI Technologies*	*SS8: Electromagnetic Modeling, Design, and Measurement of Circuits, Devices, and Metamaterials*	*SS9: ESD/EMI Techniques for Electronic Systems*	
	11:40	**Lunch**			
	END				

KEYNOTE SPEECHES I

TITLE	**Interconnect Device Modeling and Optimization with Physics-Informed Machine Learning**
TIME	9:00 – 9:40, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Jianming Jin

ABSTRACT:
Robust optimization of interconnect devices has been challenging because of the complicated electromagnetic behavior of the devices. A wide variety of optimization techniques have been proposed in the past, including search-based and gradient-based methods. All these optimization techniques are based on efficient forward solutions, which is particularly true for the search-based optimization which requires the evaluation of many designs. In the gradient-based optimization, one not only needs to provide forward solutions, but also their gradients with respect to design parameters, which are difficult to obtain. To overcome these challenges, we propose a hybrid algorithm enhanced with a machine learning approach. The hybrid algorithm combines the slow-but-global search-based method with the fast-but-local gradient descent method. To facilitate the proposed optimization scheme and improve its efficiency, we use a neural network-based surrogate model in both search and gradient descent processes. The neural network model can speed up the forward evaluation and provide analytical gradients using standard back-propagation in a very fast and accurate manner. To alleviate the computational burden associated with the time-consuming generation of training data, we further propose the use of a physics-informed machine learning model to improve modeling efficiency and reduce the training data generation cost.

BIOGRAPHY

Jian-Ming Jin is Y. T. Lo Chair Professor in Electrical and Computer Engineering and Director of the Electromagnetics Laboratory and Center for Computational Electromagnetics at the University of Illinois at Urbana-Champaign. He also serves as the Executive Dean of Zhejiang University-University of Illinois at Urbana-Champaign Institute. He has authored The Finite Element Method in Electromagnetics, Electromagnetic Analysis and Design in Magnetic Resonance Imaging, and Theory and Computation of Electromagnetic Fields, and co-authored Computation of Special Functions, Finite Element Analysis of Antennas and Arrays, and Fast and Efficient Algorithms in Computational Electromagnetics. He was elected by ISI among world's most cited authors in 2002. He is a Fellow of IEEE, OSA, ACES, and Electromagnetics Academy.

KEYNOTE SPEECHES II

TITLE	**Narrowing the Gap Between Theoretical Research and Real-world Practice for EM Engineering**
TIME	9:40 – 10:20, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Yihong Qi

ABSTRACT:
This keynote talks about the innovations from theoretical discovery of shared impedance noise coupling mechanism to real-world engineering applications, covering antenna, MIMO measurement, high speed connector, and wireless intelligent sensing, Practical examples and products are discussed.

BIOGRAPHY
Dr. Yihong Qi is an engineer, scientist, inventor, and entrepreneur. He founded Pontosense Inc., Mercku Inc., LinkE Inc., and General Test Systems. Additionally, he serves as an adjunct professor at the EMC Laboratory, Missouri University of Science and Technology, USA, and Western University, Canada. From 1995 to 2010, he worked at Research in Motion (Blackberry) in Waterloo, ON, Canada, where he was the Director of Advanced Electromagnetic Research.

Dr. Qi holds over 500 granted and pending patents and has authored more than 150 scientific papers. His multi-band smart antenna technology, which positions the antenna at the bottom of mobile terminals, significantly reduces radio-wave radiation to the human head. This innovation has protected billions of smartphone users from potential electromagnetic hazards and addressed hearing aid compatibility issues, benefiting over 20 million users who rely on hearing aids. His antenna invention has become a mainstream solution for smartphones. Furthermore, his Radiated Two Stage MIMO throughput OTA measurement international standards inventions have streamlined the certification process for 5G, intelligent connected vehicles, and the Internet of Things. He also invented the O-shaped board-to-board spring connector, which is widely used in the electronics industry with over 50 billion units produced. His high-speed connector invention showcases leading performance for next-generation high-speed interconnects for computational servers and AI computation center. His wireless intelligent sensing innovation is the first mmWave wireless sensor used for child presence detection and driver monitoring in the automotive industry, and it is also applied in elderly care, health, and medical fields, earning multiple international awards.

Dr. Qi is a distinguished lecturer for the IEEE Antenna and Propagation Society and the IEEE EMC Society. He has received the IEEE EMC Society Technical Achievement Award. His inventions have garnered multiple accolades, including three CES Innovation Awards, the CES Network Product of the Year Award, the CES Wellness Product of the Year Award, and three Red Dot Awards among other awards. He contributes to the 3GPP and CTIA international standards. Dr. Qi is a Fellow of the IEEE, the Canadian Academy of Engineering, and the National Academy of Inventors.

KEYNOTE SPEECHES III

TITLE	**Collaborative Design Optimization of Advanced Packaging and High-Density Interconnection (先进封装和高密互连的协同设计优化)**
TIME	10:40 – 11:20, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Boping Wu

ABSTRACT:
In today's complex integrated circuit design environment, the high-density interconnect design together with high computing power chips is the key to industry development. This talk discusses an advanced cross process design simulation platform and toolchain, realizing the research and development process of integrated analysis of multiple physical fields including electric field, magnetic field, force, and heat. This multi-scale and multi-media collaborative development method supports various hybrid designs and promotes the integrated development of heterogeneous integration technology. Applied in the packaging technology, the overall performance of chips can be improved, power consumption reduced, and quality reliability enhanced by integrating physical constraints and collaborative parameter optimization technology of microsystem architecture.

在当今复杂的集成电路设计环境中，大算力芯片的高密互连设计协同是行业发展的关键。本报告将介绍一种先进跨工艺的设计仿真平台和工具链，实现电、磁、力、热多物理场融合分析的研发流程。这种多尺度、多介质的协同开发方法支持各种混合设计，推动了异质集成技术的一体化发展。在封装技术应用中，通过整合物理约束和微系统架构的协同参数优化技术，提高了芯片整体性能，降低了功耗，增强了质量可靠性。

BIOGRAPHY

PhD from the University of Washington (Seattle), Vice President of JCET Group, and General Manager of Design Service Business Unit. Previously responsible for chip hardware system design and product development in multiple multinational renowned semiconductor companies.

吴伯平，美国华盛顿大学(西雅图)博士，长电科技集团副总裁，设计服务事业部总经理。曾在多家跨国知名半导体公司负责芯片硬件系统设计和产品开发。

KEYNOTE SPEECHES IV

TITLE	**Development of Multiphysics Fully Coupled Solver Applied for Simulating 3D High-Density and Ultra-wide Band Interconnects (3D 高密度和超宽带互连多物理场全耦合求解器开发)**
TIME	11:20 – 12:00, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Wen-Yan Yin

ABSTRACT:

The urgency of independently developing a 3D high-density and ultra wideband interconnected multi physics field fully coupled solver.

Key technologies in the independent development of a 3D high-density and ultra wideband interconnected multi physics field fully coupled solver.

Typical Application Demonstration of 3D High Density and Ultra Wideband Interconnected Multi Physical Field Fully Coupled Independently Developed Solver.

- 3D 高密度和超宽带互连多物理场全耦合求解器自主开发的迫切性。
- 3D 高密度和超宽带互连多物理场全耦合求解器自主开发中关键技术。
- 3D 高密度和超宽带互连多物理场全耦合自主开发求解器典型应用示范。

BIOGRAPHY

Dr.Yin obtained a doctoral degree from Xi'an Jiaotong University in 1994, previously served as a professor at Shanghai Jiao Tong University, and has been a distinguished professor at Zhejiang University since January 2009; Formerly served as a specially appointed expert of the Expert Committee of the "China Information and Electronic Engineering Technology Development Strategy Research Center" of the Chinese Academy of Engineering. Served as the Deputy Editor in Chief of IEEE T-CPMT Transactions for a long time, and was selected as an IEEE Fellow by IEEE in 2013. Published over 300 papers in IEEE Transactions and Letters, and has won awards such as the Second Prize for National Technical Invention, the Second Prize for National Science and Technology Progress, the Second Prize for National Defense Technical Invention, and the First Prize for Shanghai Science and Technology Progress.

94 年获西安交通大学博士学位，曾任上海交通大学教授，09 年 1 月至今任浙江大学求是特聘教授；曾任中国工程院“中国信息与电子工程科技发展战略研究中心”专家委员会特聘专家等。长期担任 IEEE T-CPMT 汇刊副主编，13 年被 IEEE 遴选为 IEEE Fellow。在 IEEE 汇刊和快报中发表论文 300 余篇，曾获国家技术发明二等奖、国家科技进步二等奖、国防技术发明二等奖和上海市科技进步一等奖等奖项。

INDUSTRY PLENARY I

TITLE	**CMOS mm-Wave Phased Array Design**
TIME	14:00 – 14:25, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Kai Kang, University of Electronic Science and Technology of China

ABSTRACT:

Since mm-wave frequency bands are adopted in 5G communications, CMOS mm-wave circuits and systems attract tremendous attentions because of its low cost and high integration capability. However, circuits designers have to face many challenges of CMOS process, such as the high loss substrate, low Q passive devices, high noise, and limited gain and output power. This paper will introduce technique to overcome these difficulties to design high performance wideband building blocks as well as transceiver chipsets for 5G communication.

BIOGRAPHY

Kai Kang received the B. Eng degree from the Northwestern Polytechnical University, China in 2002, and the joint Ph.D. degree from the National University of Singapore, Singapore and Ecole Supérieure D'électricité, France in 2008. Dr. Kang was with the Institute of microelectronics, A*STAR, Singapore as a Senior Research Engineer, and with Global foundries as a Principle Engineer, respectively. Since June 2011, he has been a professor at the University of Electronic Science and Technology of China. His research interests are RF and RF & mm-Wave integrated circuits design and modeling of on-chip devices.

Dr. Kang has authored and co-authored over 200 international referred journal and conference papers, and was co-recipient of several best paper awards or best student paper awards in IEEE conference including Silkroad award in ISSCC 2018. He received the National Science Fund for distinguished young scholars.

INDUSTRY PLENARY II

TITLE	**AI-driven Signal Integrity Analysis for Accurate and Faster Designs**
TIME	14:25 – 14:50, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Kezhou Li, Cadence

ABSTRACT:

In the 5G and 6G communications era, signal integrity design considerations have become increasingly crucial in high-speed interface design. Interconnects in the PCB and the package carry high-speed signals around the board and must be designed to eliminate common signal integrity problems. The design process usually relies heavily on human intuition, but with the help of a few AI applications, the engineer can increase design productivity by 75X.

BIOGRAPHY

Kezhou Li is an enthusiast in electromagnetics simulation with 15+ years of experience and a director in Cadence's Multi-Physics System Analysis (MSA) division, leading the product engineering/verification team in China. He witnesses the growth of Cadence in the system simulation domain and defines the roadmap of flagship tools in the electronic simulation domain.

INDUSTRY PLENARY III

TITLE	**Challenges and Solutions for PCB Manufacturing in 224G Applications (224G 应用下 PCB 制造的挑战及应对方案)**
TIME	15:05 – 15:30, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Xuechuan Han, Shennan Circuits Co., Ltd.

ABSTRACT

Due to the AI wave, the amount of data has surged and the need for efficient data transmission has increased dramatically. It is an inevitable trend to increase the signaling rate of a single channel. It is expected that single-channel 224G solutions will see deployment uptake in 2026. Due to the increased rate, 224G solutions face higher challenges in terms of loss, return loss, and crosstalk. For SerDers, chip packaging, PCB, connectors and other components have put forward higher requirements.

Facing the challenges of 224G in terms of loss, vias bandwidth, crosstalk, etc., the enhancement of PCB processing capability is especially critical, and the brownout process, stub length control, vias size, layer bias control, impedance control, etc. have a key impact on the signal integrity of 224G. This report analyzes the challenges faced by 224G on the PCB side, and shows the solutions we have already accomplished or are working on for these challenges.

由于 AI 浪潮的推动，数据量激增，数据的高效传输的需求也大幅增加。提升单通道的信号传输速率是必然趋势。预计单通道 224G 的方案将在 2026 年迎来部署上量。由于速率的提升，224G 方案在损耗、回损、串扰等方面面临更高的挑战。对于 SerDers、芯片封装、PCB、连接器等各个组件均提出了更高的要求。

面对 224G 在损耗、过孔带宽、串扰等方面的挑战，PCB 加工能力的提升尤为关键，棕化工艺，stub 长度控制，孔盘尺寸，层偏控制，阻抗控制等方面对 224G 信号完整性有关键的影响。本报告浅析 PCB 端 224G 面临的挑战，本针对这些挑战，展示我们已经完成或正在进行的解决方案。

BIOGRAPHY

Xuechuan Han, Director of Product R&D of Shennan Circuits Co., Ltd. He mainly engaged in PCB key technology mechanism research, model construction, new products and technology research, promotion to batch application, for the company's insight into new business opportunities and directions, the ability to reserve new products and technologies in advance, as well as the key technical capabilities to enhance and optimize.

韩雪川，深南电路股份有限公司产品研发总监，主要从事 PCB 关键技术的机理研究、模型建设以及新产品新技术的研发、推广到批量应用，为公司洞察新的业务机会和方向、提前储备新产品技术的能力以及关键技术能力的提升和优化。

INDUSTRY PLENARY IV

TITLE	**Improvements in Simulation and Test Accuracy for 56G PAM4 System**
TIME	15:30 – 15:55, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Jianguo Zhang, Sanechips

ABSTRACT

In this paper, the TDR impedance and eye diagram of the 56G PAM4 system are simulated and measured through a practical case, and the accuracy of less than 5% is finallyobtained. Several key factors affecting the accuracy of simulation and testing are discussed in detail, which will be guiding significance for the 112G and 224G serdes system SI simulation work

BIOGRAPHY

SIPI Simulation Level 5 Expert, Chengdu Packaging Leader, Sanechips.

张建国，中兴微电子 SIPI 仿真 5 级专家，成都封装负责人。

INDUSTRY PLENARY V

TITLE	**Roughness Variation after Etching and Its Influence to Loss Up to 90GHz**
TIME	15:55 – 16:20, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Rongyao Tang, Fiberhome Communication Technology Co.

ABSTRACT

With the increasing demand for optical modules driven by 5G communication and AI computing, the signal channel from DSP chip to optical devices will exceed 130Gbaud/s, requiring a 3dB bandwidth of over 70GHz. Accurately and quickly estimating high-frequency losses in the channel poses a significant challenge.

The slides discuss a case study done on roughness variation after etching and its influence to loss up to 90GHz.

BIOGRAPHY

Rongyao Tang, Interconnection Technologist, Fiberhome Communication Technology Co.

汤荣耀，烽火通信互连技术专家

INDUSTRY PLENARY VI

TITLE	**System Integration Impact on SI**
TIME	16:20 – 16:45, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Yinglei Ren, Intel

ABSTRACT

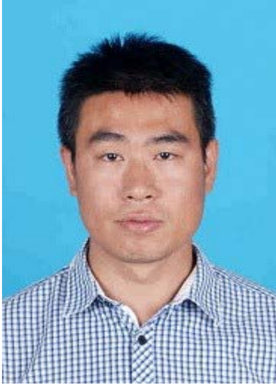
As signal speed becomes higher, every design detail count. Signal performance is not only related with the channel design itself, but also impacted by system integration (e.g. power noise, thermal solution, mechanical part etc.). In this session, the presenter will share how system integration impacts SI performance with examples. More and more cross-domain co-optimization will be needed in future designs.

BIOGRAPHY

Yinglei Ren is a signal integrity engineer from Intel Data Center and AI group, focusing on high-speed signal design optimization and system integration. She joined Intel in 2005 after graduating from Shanghai Jiao Tong University with M.S.E.E. and B.S.E.E. degrees.

INDUSTRY PLENARY VII

TITLE	**112Gbps Signal Integrity Design Key Points**
TIME	16:45 – 17:05, November 6th
VENUE	Pacific Hall @Level 1
SPEAKER	Zhenwei Zhao, Dawning Information Industry Co., Ltd



ABSTRACT

In this paper，discussing the 112Gbps 4-pulse amplitude modulation signal integrity design key points, including 1. chip ballmap design, 2. PCB via optimize, Impence control, insertion loss and crosstalk control, power noise, PCB new technology. 3. System copper cable using in 112G high speed system.

BIOGRAPHY

Zhenwei Zhao, System Architect & SIPI Simulation Expert, Director Engineer, Dawning Information Industry Co., Ltd

赵振伟，中科曙光 系统架构师 & SIPI 仿真专家，主任工程师。

Technical Sessions – Thursday, NOVEMBER 7, 2024

Room	Room #1 JiangNan Function Room	Room #2 YuanShi Function Room	Room #3 JuXian Function Room	Room #4 XinHui Function Room
	SS1: Advanced SI Modeling, Design, and Testing Technologies	**SS2: Advanced PI and Multiphysics Modeling, Design, and Testing Technologies**	**SS3: ESD Techniques for Integrated Circuits and Electronic Systems**	**Abstract Session (Poster Discussion)**
SESSION CHAIR	***Xiaohe Chen,*** *China University of Petroleum, Beijing* ***Shufang Li,*** *Beijing University of Posts and Telecommunications*	***Huapeng Zhao,*** *University of Electronic Science and Technology of China* ***Siping Gao,*** *Nanjing University of Aeronautics and Astronautics*	***Shurong Dong,*** *Zhejiang University* ***Fayu Wan,*** *Nanjing University of Information Science and Technology*	
08:40-09:10	Equivalent Electromagnetic Modeling based on Measurement-Computation Fusion *(Huapeng Zhao, University of Electronic Science and Technology of China)*	Advanced Discontinuous Galerkin Method for the Multiphysics Computation of High-Power Microwave Waveguides *(Ping Li, University of Electronic Science and Technology of China)*	High Voltage and High Immunity ESD Protection Design(高压、高抗扰ESD防护设计) *(Dawei Lai, Weixin Technology (Xuzhou) Co., Ltd)*	Abstract Session (Poster Discussion)
09:10-09:40	An Improved 1X De-embedding Method *(Xing-Chang Wei, Zhejiang University)*	Power Delivery of Chiplets: Challenges and Opportunities *(Siping Gao, Nanjing University of Aeronautics and Astronautics)*	The ESD and EOS Integrated Protection on Chip for Improving the IC Reliability. *(Hailian Liang, Jiangnan University)*	Abstract Session (Poster Discussion)
09:40-10:10	Medical Device Electromagnetic Compatibility: Design Challenges and solutions (医疗器械电磁兼容设计挑战与应对) *(Xiaohe Chen, China University of Petroleum, Beijing)*	Machine Learning Assisted SI/PI Modeling and Optimization *(Ling Zhang, Zhejiang University)*	Investigation on Fabrication-induced High-leakage Issue of an Overdrive ESD Power Clamp in Advanced FinFET Technology *(Guangyi Lu, Southeast University)*	Abstract Session (Poster Discussion)
10:10-10:40	Signal Integrity Modeling and Anlysis Method for Neuromorphic Chips (智能类脑芯片信号完整性建模与分析) *(Hanzhi Ma, Zhejiang University）*	Innovative PDN Design Using Equivalent Circuits for Enhanced Power Integrity Beyond Decoupling Capacitors *(Zhifei Xu, DeTooLIC Technology)*	Cable Discharge Event Evaluation Methods Discussion *(Bingsheng Gao, ESDEMC Technology)*	Abstract Session (Poster Discussion)
11:00-11:30	Efficient and Reliable Full-wave Finite Element EM Solvers for Real-life Signal Integrity Applications *(Wei Wang, Hangzhou Dianzi University)*	**Panel Discussion I (EDA for High Speed and High Bandwidth Interconnects)**	Research on ESD Protection Technology for RF SOI MOS RF Switch Array *(Shurong Dong, Zhejiang University)*	
11:30-12:00		**Panel Discussion I (EDA for High Speed and High Bandwidth Interconnects)**		

	SS4: EMC Techniques for Integrated Circuits	**SS5: Advanced EMI Modelling and Measurement Technologies**	**SS6: Signal/Power Integrity and Multiphysics Analysis for Chiplets**	**Award Ceremony**
SESSION CHAIR	***Qiang Cui,*** *China Electronics Standardization Association* ***Jianfei Wu,*** *Tianjin Institute of Advanced Technology*	***Xing-Chang Wei,*** *Zhejiang University* ***Da Yi,*** *Chongqing University*	***Bo Pu,*** *DeTooLIC Technology* ***Wenchao Chen,*** *Zhejiang University*	
13:30-14:00	Thoughts on Forward Design Technology for Electromagnetic Compatibility and Protection of Chips/Boards *（Zhaowen Yan, Beihang University）*	Failure Mechanism and Electromagnetic Compatibility Design of Digital Control Circuit in Mixed Electromagnetic Environment *(Henglin Chen, Zhejiang University)*	Machine Learning-Assisted Modeling and Simulation of Chiplet Based High Speed IOs *(Cheng Zhuo, Zhejiang University)*	Award Ceremony
14:00-14:30	Research and Practical Cases on Electromagnetic Compatibility Testing Technology for Automotive Chips (车规芯片电磁兼容测试技术研究及实际案例) *(Qiang Cui, China Electronics Standardization Association)*	A Method of Analyzing the Impact of the Wiring Parameters on the Electromagnetic Coupling to PCB Inside Electronic Equipment *(Pei Xiao, Hunan University)*	Crosstalk Cancellation Circuit Design Techniques for High-Density and High-Speed Interconnects *(Yuan Du, Nanjing University)*	Award Ceremony
14:30-15:00	Near Field Scanning Techniques for IC *(Wenxiao Fang, Sun Yat-sen University)*	EMI Simulation and Analysis Between Active Chips Within Shared Shielding Can *(Da Yi, Chongqing University)*	Exploration of Multi-physics Modeling and Intelligent Technologies *(Qiwei Zhan, Zhejiang University)*	Award Ceremony
15:00-15:30	Multi-physical Field Coupling Characteristics of IC Pins Distribution on High-frequency Flexible PCB *(Mengjun Wang, Hebei University of Technology)*	A Convolutional Neural Network-Based Method for Modeling Electromagnetic Interferenced Image Sensor *(Qibo He, OPPO)*	Multiphysics and Nonlinearity Modeling/Measurement of RF Interconnects *(Wenchao Chen, Zhejiang University)*	
15:30-16:00	Study on Electrostatic Discharge Sensitivity of Integrated Circuits *(Xiaojun Hu, 3C Test)*	Research on the Principles and Applications of Filtering Cables for Protection in Complex Electromagnetic Environments *(Yunan Han, Beijing University of Chemical Technology)*	Exploring EDA Tools for Collaborative Design and Simulation of 2.5D/3D ICs in Advanced Packaging *(Yi Zhao, Zhuhai Silicon Chip Technology Ltd.)*	
16:20-16:50	Mechanism of Multi-physical Field Effects in RF CMOS Circuits and MEMS Devices *(Shitao Chen, Anhui University)*	Evaluation of Non-linear Characteristic of Magnetic Core for Compact EMI Filter Design *(Anfeng Huang, DeTooLIC Technology)*	Evolution and Prospect of High-Density Chiplet Integration Technology *(Shujuan Liu, Yangtze Laboratory)*	**Panel Discussion II (Solutions and Trends of High-Speed Cables and Connectors)**
16:50-17:20		*Electromagnetic Compatibility Issues of Neuromorphic Chips and Heterogeneous Integrated Circuits* *(Yan Li, China Jiliang University)*	Research on the Reliability of 2.5D/3D IC under Multi Physical Field Coupling *(Jiahao Zhou, DeTooLIC Technology)*	**Panel Discussion II (Solutions and Trends of High-Speed Cables and Connectors)**

Technical Sessions – Friday, NOVEMBER 8, 2024

Rooms	**Room #1** JiangNan Function Room	**Room #2** YuanShi Function Room	**Room #3** JuXian Function Room
	SS7: AI Assisted EMC/SI/PI Technologies	**SS8: Electromagnetic Modeling, Design, and Measurement of Circuits, Devices, and Metamaterials**	**SS9: ESD/EMI Techniques for Electronic Systems**
SESSION CHAIR	***Xiuqin Chu,*** *Xidian University* ***Hanzhi Ma,*** *Zhejiang University*	***Xiong Chen,*** *Xi'an Jiaotong University* ***Ling Zhang,*** *Zhejiang University*	***Shurong Dong,*** *Zhejiang University* ***Fayu Wan,*** *Nanjing University of Information Science and Technology*
08:30-09:00	A Comprehensive Design Methodology for Chiplet-Based 2.5-D Integrated Circuits *（Wensheng Zhao, Hangzhou Dianzi University）*	Progess in the Development of Silicon-Based Terahertz Radiation Sources and Phased Array Chips *（Liang Gao, Southeast University）*	Charged Device Model ESD Sensitivity Tester Design and Application *(Fayu Wan, Nanjing University of Information Science & Technology)*
09:00-09:30	Computer Vision Assisted Metamaterial Systems for Self-Adaptive Wireless Communications *(Wenxuan Tang, Southeast University)*	Seeking Shapes of Planar Interconnects with Higher Flexibility *（Xiaojie Ma, Beijing Huairou Laboratory）*	Review and Case Study of ESD Simulation *(Qiang Cui, Zhejiang University's College of Integrated Circuits)*
09:30-10:00	Space Mapping Techniques for EM Design Optimization *（Feng Feng, Tianjin University）*	Preliminary Conceptual Study of Novel Materials, Devices and Test Equipments for Electromagnetic Compatibility *（Yusheng Hu, Jimei University）*	Modeling the Transmission Characteristics of ESD Signal in a Non-linear System *(GuangXiao Luo, North China Electric Power University)*
10:00-10:30	Machine Learning-Enabled Fast Electromagnetic Modeling and Optimization Approaches to Metasurface Design *（Jianan Zhang, Southeast University）*	Analysis of Power Device Switching Characteristics and EMI Optimization of Motor Drivers *(Yongning He, Xi'an Jiaotong University)*	EMI Issues and Challenges in Consumer Electronics *（Kaixiang Zhu, Honor Device Co., Ltd）*
10:40-11:10	High-Speed Circuit Transient Simulation based on Machine Learning Techniques *(Hanzhi Ma, Zhejiang University)*	Evaluation Method for Roughness Performance of Copper Foil *(Yade Fang, DeTooLIC Technology)*	Study on Radiation Interference from High-Speed Railway Pantograph-Catenary Detachment arc Considering the Train Speed Influence *(Ke Huang, Southwest Jiaotong University)*
11:10-11:40	Application of Machine Learning in Signal Integrity *（Xiuqin Chu, Xidian University）*	Capacitance Impact on Passive Intermodulation Generation with its Measurement *（Xiong Chen, Xi'an Jiaotong University）*	

ABSTRACT SESSION (POSTER DISCUSSION)

TITLE	AUTHORS	AFFILIATION
3–100 GHz Flexible Substrate Integrated Suspended Line with Air Cavity	*Li Yu-Rou, Wang Meng-Jun*	*Hebei University of Technology*
Design of High-Robustness SCR Incorporating Parasitic BJT for High-Voltage ESD Protection	*Yujie Liu, Xiangliang Jin*	*Hunan Normal University*
A Novel Phaseless Dipole Source Reconstruction by Leveraging Framework of Neural Network	*Dong-Hao Han, Xing-Chang Wei*	*Zhejiang University*
Evaluation of Impact of Parasitism on De-Embedding	*Si-Yao Tang, Xing-Chang Wei*	*College of Information Science, Electronic Engineering, Zhejiang University*
The Standard Deviation of Dynamic Voltage Noise	*Haiyue Yuan, Yuhuan Luo, Tao Wei, Yuhao Huang, Xiuqin Chu, Jun Wang, Feng Wu,*	*Xidian University*
Calculation Method for Worst-case Power Supply Noise in Multi-chip Systems	*Yuhuan Luo, Haiyue Yuan, Tao Wei, Yuhao Huang, Xiuqin Chu, Jun Wang, Feng Wu*	*Xidian University*
Computation Method for Differential Skew Based on Variational Method	*Yan Xu, Huailong Zhang, Aobo Li, Haiyue Yuan, Yuhuan Luo, Jun Wang, Xiuqin Chu*	*Xidian University*
Deep Reinforcement Learning Routing Algorithm Considering Signal Integrity	*Kangkang Zhang, Huailong Zhang*	*Xidian University*
Enable UCIe Interconnection Beyond Standard Specification	*Chenghai Yan, Ramaswamy Parthasarathy, Harrison Xue, Chuanyu Li, Nikita Ambasana, Yinglei Ren*	*Intel Corporation*
Random Jitter Amplification Coefficient Calculation Based on Phase Noise	*Tao Wei, Yuhao Huang, Haiyue Yuan, Yuhuan Luo, Jun Wang, Xiuqin Chu*	*Key Laboratory of High-Speed Circuit Design and EMC Ministry of Education*
Improvements in simulation and test accuracy of eye diagram and TDR impedance for 56G PAM4 System	*Jianguo Zhang, Xia Ming, Liguangyao*	*Sanechips*
Deep Reinforcement Learning for Decoupling Capacitor Optimization in PCB Power Delivery Networks	*Qiyu Jiang, Shufang Li*	*Beijing University of Posts and Telecommunications*
A Novel Fast Analysis Method for High-Speed Link Errors	*Yuhao Huang, Tao Wei, Haiyue Yuan, Yuhuan Luo, Xiuqin Chu, Jun Wang, Feng Wu*	*Xidian university*
Electro-Thermal Modeling of Spoof Surface Plasmon Polariton Transmission Line	*Zehao Zheng, Min Tang, Junfa Mao*	*Shanghai Jiao Tong University*
Modeling and Experimental Analysis of the Influence of Bonding Wires Layout on Chip Surge Capability	*Feilin Zheng, Chao Zheng, Xuebao Li, Xiang Cui*	*north china electric power university*
A Design Method for Shielded Structure of Cable Based on Artificial Neural Network Algorithm	*Xiaotian Chen, Shengchao Peng, Jinpeng Li, Pei Xiao, Gaosheng Li*	*Hunan University*
A Novel PPO-Based Method for Automatically Designed EBG Structure	*Bing-Han Xie, Xiao-Chun Li*	*Shanghai Jiao Tong University*

FDFD simulation of nonlinear effects in BAW filters	*Xiaolong Zhao, Zixia Yu*	*Xi'an Jiaotong University*
Symmetrical Gradient Cascaded Low-pass Filtering Cable Based on Unbalanced Rectangular Structures	*Tian-le Yu, Yu-nan Han*	*Beijing University of Chemical Technology*
Design of Bandpass Filter Using Coaxial Defected Conductor Structures	*Meng-yao Cai, Yu-nan Han*	*Beijing University of Chemical Technology*
Shielding Effectiveness Measurement of Form-in-place Gasket by Cavity-to-cavity Test Method	*Aqiao Jin, Yunan Han*	*Beijing University of Chemical Technology*
Efficient E-T Simulation	*Hangkai Zhang*	*Zhejiang University*
Modeling the transmission characteristics of ESD signal for a TVS-included non-linear system	*Shuo-jie Li, Yang Zhao, Jian-Fang Dang, Jie Gao, Bao-Cheng Huang, Guang-Xiao Luo*	*North China Electric Power University (Baoding)*
Study on the Transient Conducted Coupling Mechanism Between the Power and IO Ports of Digital Control Circuit	*Yang Xiao, Zhongyuan Zhou, Jinjing Ren*	*Information Engineering University*
Research on the Distributed Parameter Matrix of Interconnected Cable Based on MoM	*Yixing Gu, Zhongyuan Zhou, Mingjie Sheng*	*Research Center for Electromagnetic Environmental Effects, School of Mechanical Engineering, Southeast University*
A Comprehensive Design Methodology for Chiplet-Base 2.5-D Integrated Circuits	*Peng Zhang, Da-Wei Wang, Wen-Sheng Zhao*	*Hangzhou Dianzi University*
Localized Capacitance Extraction for Interconnects in Finite-sized Layered Medium	*Yangzheng Yuan, Linsong Huang, Huapeng Zhao*	*University of Electronic Science and Technology of China*
A Comparative Study of Different Excitation Methods for High Contrast Magnetic Material Modeling Using PEEC Method	*Xiaoping Li, Xu Wang, Qiusen He, Jun Fan*	*Southwest University of Science and Technology*
A Decoupling Capacitor Optimization Method for PSIJ and Transient Noise Reduction	*Li Jiang, Ling Zhang, Er-Ping Li*	*Zhejiang University*
Multi-Port Interconnect Parasitic Parameter Extraction Tool Bsed on Fast Direct PEEC	*Linsong Huang, Chunhua Wu, Huapeng Zhao*	*University of Electronic Science and Technology of China*
A Method for RLCG Parameter Extraction of Multi- Stranded Wires Based on PSO-BP Neural Network	*Guanghao Liu, Ying Wang, Jian Wang*	*Ningbo University*
A Novel Connector Design for PCIe Gen6	*Lei Deng, Yinzhu Tang, Qingfeng Lin*	*LinkE Technologies Co., Ltd; Hunan University*
Design of MIMO Planar Sparse Array and Improved Back-Projection Algorithm for High-Performance 3-D Microwave	*Yuke He, Kuiwen Xu*	*Hanzhou Dianzi University*

Physical inspired quantitative computational imaging with limited aperture	*Yuxin Zhang, Kuiwen Xu*	*Hangzhou Dianzi University*
Advanced RF Probe Calibration Algorithm and Calibration Standard Definition Method for Broadband S-parameter Measurement	*Jiefeng Zhou, Ziyang Chen, Wendi Li, Ling Zhang, Er-Ping Li*	*Zhejiang University*
Smart Surface Defect Detection Method on Cable Coating using Intermodulation Index	*Tianyu Zhuang, Zhiyuan Feng, Xiong Chen*	*Xi'an Jiaotong University*
Capacitance Impact on Passive Intermodulation Phase with Its measurement	*Zhiyuan Feng, Xiong Chen*	*Xi'an Jiaotong University*
Deep Simple Recurrent Unit based Neural Equalizer for High-Speed Links	*Jiarui Qiu, Zengyi Sun, Hanzhi Ma, Er-Ping Li*	*Zhejiang University*
Compact Model of Diffusive Memristor Device for Neuromorphic Computing	*Yining Jiang, Hanzhi Ma, and Er-Ping Li*	*Zhejiang University*

OVERVIEW OF SESSIONS I

SESSIONS	Advanced SI Modeling, Design, and Testing Technologies
VENUE	Room 1: JiangNan Function Room @Level 2（2 楼江南厅）
TIME	08:40-11:30 November 7th
SESSION CHAIR	Xiaohe Chen, China University of Petroleum, Beijing Shufang Li, Beijing University of Posts and Telecommunications
INVITED TALK	**Equivalent Electromagnetic Modeling based on Measurement-Computation Fusion** *Huapeng Zhao, University of Electronic Science and Technology of China* **An Improved 1X De-embedding Method** *Xing-Chang Wei, Zhejiang University* **Medical Device Electromagnetic Compatibility: Design Challenges and Solutions** **(医疗器械电磁兼容设计挑战与应对)** *Xiaohe Chen, China University of Petroleum, Beijing* **Signal Integrity Modeling and Anlysis Method for Neuromorphic Chips** **(智能类脑芯片信号完整性建模与分析)** *Hanzhi Ma, Zhejiang University* **Efficient and Reliable Full-wave Finite Element EM Solvers for Real-life Signal Integrity Applications** *Wei Wang, Hangzhou Dianzi University*

TITLE	**Equivalent Electromagnetic Modeling based on Measurement-Computation Fusion**
TIME	08:40-09:10 November 7th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Huapeng Zhao, University of Electronic Science and Technology of China

ABSTRACT

Equivalent electromagnetic modeling is useful for solving complex engineering problems. This talk will share the speaker's recent work on equivalent electroamgentic modeling, especially equivance based on measurement-computation fusion. The talk consists of three parts.

First, integrated simulation of antennas on electrically large platforms will be dicussed. Sparse equivalent source model of antennas is extracted by field decomposition and source tracing. Utilizing sparsity of source model, the constraint on near field samples is broken, and the near field scanning effort is saved. Moreover, it is shown that the equivalent source model of anntenas effectively overcome ill-conditioning of system matrix for multi-scale simulation, and thus reduces integrated simulation time and memory costs.

Second, in order to capture evanescent modes in near field, near field transformation based on integral equation (IE) is investigated. The computation complexity of integral equation is reduced by 2~3 orders by a specifically designed fast algorithm. It is shown that the IE based on fast algorithm can ahcieve similar computation speed as the popular mode-based algorithm, while accurately capturing the evanescent modes ignored by mode-based algorithm, which paves an effcient and accurate way of electromagnetic analysis based on near field measurement.

Third, for circuit-level equivalent modeling, an equivalent circuit extraction tool is developed based on fast direct partial element equivalent circuit (FDPEEC) method. A fast matrix filling and invsion method is developed based on low-rank compression and by utilizing the special structure of PEEC system matrix. The FDPEEC method is especially useful for the equivalent modeling of a large number of interconnentcs, for

which case FDPEEC is more efficient than FastCap and FastHenry developed by MIT. The FDPEEC-based tool can be used together with behavior model of chips for high-level modeling and simulation.

BIOGRAPHY

Dr. Huapeng Zhao received the Ph.D. degree from Nanyang Technological University, Singapore, in June 2012. He was a Scientist with the A*STAR Institute of High Performance Computing, Singapore, from August 2011 to December 2015. Since December 2015, he has been with the University of Electronic Science and Technology of China, Chengdu, China, first as an Associate Professor, and promoted to a Full Professor in May 2021. He has authored or coauthored over 150 technical papers published in international journals or conferences. His current research interests include system-level electromagnetic analysis and design, and signal and data processing techniques in electromagnetics. Prof. Zhao received the IEEE APEMC Young Scientist Award and the URSI Young Scientist Award. He is currently a Young Editorial Board Member of Electromagnetic Science, and an Associate Editor of IEEE AWPL.

TITLE	**An Improved 1X De-embedding Method**
TIME	09:10-09:40 November 7th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Xing-Chang Wei, Zhejiang University

ABSTRACT

The conventional 1X de-embedding method based on time-domain reflectometry (TDR) loses accuracy when there are impedance discontinuities at the terminal of fixtures. To address this issue, this study proposes an improved 1X de-embedded method. By connecting an extension line to the terminal of the fixture, which is used as an OPEN_EX standard, the proposed method precisely identifies peaks resulting from the impedance discontinuities at the terminal, thereby accurately reconstruct the S_{11} and S_{22} of the fixture. The proposed method is performed on numerical and measurement examples and demonstrates higher accuracy, while keeping the same efficiency as the traditional 1X method.

BIOGRAPHY

Xing-Chang Wei (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Xidian University, Xi'an, China, in 2001. From 2001 to 2010, he was with the Institute of High-Performance Computing, Agency for Science Technology and Research, Singapore, as a Research Fellow, Senior Research Engineer, and Research Scientist. In 2010, he joined Zhejiang University, Hangzhou, China, as a Full Professor. He authored and coauthored more than 200 papers published in prestigious international journals and conferences. His research interests include near-field scanning, power integrity and signal integrity simulation and designs.

Dr. Wei was the Associate Editor of IEEE Transactions on Electromagnetic Compatibility, Co-Chair of the Technical Program Committee of the 2010 IEEE Electrical Design of Advanced Packaging and Systems Symposium, Program Chair and TPC member of Asia-Pacific Symposium on Electromagnetic Compatibility. He was the recipient of the 2007 Singapore Institution of Engineers Prestigious Engineering Achievement Award for his contribution on the development of the reverberation chamber.

TITLE	**Medical Device Electromagnetic Compatibility: Design Challenges and Solutions(医疗器械电磁兼容设计挑战与应对)**
TIME	09:40-10:10 November 7th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Xiaohe Chen, China University of Petroleum, Beijing

ABSTRACT

With the development of electronic information technology, mobile communication devices and various electronic devices are widely used, bringing convenience to people while also making the daily electromagnetic environment increasingly complex. At the same time, in the medical field, emerging active medical devices are emerging, providing more means for disease prevention and treatment. The various types of medical electronic devices often need to cooperate with each other to jointly ensure people's life and health. Therefore, medical electronic devices must be able to operate stably in a complex electromagnetic environment. The design and verification of electromagnetic compatibility (EMC) performance of active medical devices have become increasingly important, and their design implementation also faces more challenges.

This report delves into the principles and concepts of electromagnetic compatibility, the necessity of electromagnetic compatibility design for active medical devices, difficulties, compliance, and countermeasures. It analyzes the principles of electromagnetic compatibility issues in medical electronic devices, the challenges faced in design, and methods of response. In addition, the report introduces strategies and methods for dealing with electromagnetic compatibility issues from the whole machine system to the PCB board level through several examples of electromagnetic compatibility design rectification of active medical devices. It illustrates that a technical route combining professional instrument measurement and modeling simulation analysis can efficiently achieve the analysis, positioning, and comparative verification of electromagnetic compatibility issues, providing strong theoretical and technical support for improving the electromagnetic compatibility performance of active medical devices.

BIOGRAPHY

Chen, Xiaohe: Professor at the School of Artificial Intelligence, China University of Petroleum (Beijing)

Chen Xiaohe graduated from the Department of Computer Science at Tsinghua University in 2000 with a bachelor's degree, obtained a master's degree in electronic engineering from the University of South Illinois in 2003, and received a Ph.D. in electronic engineering from the University of Missouri in 2007. From 2007, he served as the Chief System Architect in the Design Analysis and Product Blueprint Department at Apple's headquarters. The Design Analysis and Product Blueprint Department at Apple's headquarters is the company's core architectural engineering team, composed entirely of senior Ph.D. system architects from Stanford and Cornell. He participated in the product design, high-speed circuit design, production line statistical analysis, and quality control of Apple's entire product line, saving hundreds of millions of dollars in R&D costs for the company. He was involved in the formulation of international standards for Thunderbolt, Lightning, and USB3.0C.

In 2015, he returned to China and joined the Suzhou Institute of Biomedical Engineering and Technology, Chinese Academy of Sciences. During his tenure at the institute, Xiaohe served as the director of the Electromagnetic Compatibility Research Center and the head of the Medical Electronics Technology Research Office. In 2022, he was introduced as a discipline leader to the School of Artificial Intelligence at China University of Petroleum (Beijing).

Professor Chen has been engaged in electromagnetic compatibility and signal integrity research for many years, with extensive experience in system integration, high-speed circuit design, signal processing, image processing, chip design, radio frequency circuits, and computational electromagnetic field theory. He holds two US invention patents and has published dozens of scientific papers in journals such as IEEE Transactions. He has global competitiveness in the fields of electronic system integration design, artificial intelligence, signal integrity, and computer vision technology.

TITLE	Signal Integrity Modeling and Anlysis Method for Neuromorphic Chips (智能类脑芯片信号完整性建模与分析)
TIME	10:10-10:40 November 7th
VENUE	JiangNan Function Room @Level 2（2楼江南厅）
SPEAKER	Hanzhi Ma, Zhejiang University

ABSTRACT

Due to the "memory wall" problem of the traditional von Neumann architecture, efficient execution of artificial intelligence operations has become a huge challenge. Memristor-based neuromorphic chip is a typical circuit architecture of neuromorphic chips, which adopts a crossbar array structure, utilizes memristors as artificial neural synapses, and realizes signal transmission between crisscross interconnecting wires. Such chip design reduces the steps of accessing the off-chip memory when acquiring data, and simply realizes the vector matrix multiplication on the circuit level. However, due to the unstable device performance, special circuit structure, high integration and high operation speed, the reliability of the memristor-based neuromorphic chips is still poor.

At present, several circuit modeling, analysis, and design methods are being used to investigate signal integrity issues in memristor-based neuromorphic chips. Among them, the Partial Element Equivalent Circuit (PEEC) method has been widely considered and studied. This presentation will review recent progress on the application of PEEC to signal and power integrity analysis of neuromorphic chips. Furthermore, starting from the development of PEEC method in memristor-based neuromorphic chips, this presentation plans to introduce the theory of extracting parasitic parameters of neuromorphic chips by PEEC method in detail, and discusses future research opportunities.

BIOGRAPHY

Hanzhi Ma is currently an assistant professor at Zhejiang University and an adjunct assistant professor at University of Illinois Urbana-Champaign. She received the B.S. degree and Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2017 and 2022. Her research interests involve electromagnetic compatibility, signal integrity, and power integrity, with a focus on electronic automation design methods for electromagnetic integrity in high-performance integrated circuits. She has twice received the President's Memorial Award from IEEE Electromagnetic Compatibility Society and has been selected as the Young Professional Ambassador of IEEE Electromagnetic Compatibility Society. She won the Excellent Doctoral Thesis Award from Chinese Institute of Electronics and the Best Student Paper Award at the Asia-Pacific International Symposium on Electromagnetic Compatibility. She has served as a Guest Editor for IEEE Transactions on Components, Packaging and Manufacturing Technology and as a TPC member and session chair for more than 10 international conferences (including IEEE EDAPS 2020-2024, IEEE EMC Symposium 2024, APEMC 2022-2024, and ACES 2023-2024).

TITLE	Efficient and Reliable Full-wave Finite Element EM Solvers for Real-life Signal Integrity Applications
TIME	11:00-11:30 November 7th
VENUE	JiangNan Function Room @Level 2（2楼江南厅）
SPEAKER	Wei Wang, Hangzhou Dianzi University

ABSTRACT

Full-wave electromagnetic(EM) simulations play a crucial role in addressing signal integrity issues in modern electronics design and optimization. As electronic devices become increasingly compact and operate at higher frequencies, maintaining the integrity of signals becomes a significant challenge. Full-wave simulations help engineers accurately model and analyze the electromagnetic behavior of complex electronic structures, including the propagation, reflection, and interference of waves within these systems. This presentation gives a brief overview of a non-conforming, finite elements based domain decomposition (DD-FEM) framework for solving signal integrity applications. Specifically, a frequency-domain DD-FEM method based on two sets of Lagrange multipliers on the mesh interfaces will be presented, followed by some real-life numerical

studies to show that the presented DD-FEM framework is highly accurate compared with the traditional vector FEM solver and scalable with respect to mesh discretization and domain partition count. Meanwhile, we also show some potential issues of the presented framework to solve full-wave EM problems, these include its prohibitively computational overhead arising from the mathematical formulation and problematic convergence performance by using iterative solvers without proper preconditioning. Then a number of techniques for run-time acceleration, memory reduction and better convergence stability with a multi-level preconditioning scheme will be introduced, these techniques are mainly based on randomized matrix computation methods and rank-revealing algorithms which are under active development in various scientific and engineering fields including machine learning. In addition, some current technical challenges and possible solutions will be mentioned in this presentation. Finally, two real-life and challenging numerical examples are provided to show the validity, efficiency and reliability of the presented framework.

BIOGRAPHY

Wei Wang, PhD, is currently a faculty member at Hangzhou Dianzi University. Dr. Wang received his PhD degree from University of Massachusetts Amherst in 2015 under the supervision of Prof. Marinos Vouvakis. During his PhD, he worked on developing efficient and robust finite element and domain decomposition solvers for challenging multiscale electromagnetic simulations. He joined Synopsys as a senior R&D engineer after graduation and then joined Cadence Design Systems as a principal engineer, responsible for core R&D of Cadence's full-wave EM products including Clarity 3D Solver and EMX. Later he joined Meta Platforms as a research scientist working on low-level machine learning algorithms in the Reality Labs. In 2023, he joined Hangzhou Dianzi University with a full-time faculty position, his current interests include multiscale EM and multi-physical solvers, AI for engineering and hybrid modeling techniques for EMC&EMI problems.

OVERVIEW OF SESSIONS II

SESSIONS	Advanced PI and Multiphysics Modeling, Design, and Testing Technologies
VENUE	Room 2: YuanShi Function Room @Level 2（2楼院士厅）
TIME	08:40-10:40 November 7th
SESSION CHAIR	Huapeng Zhao, University of Electronic Science and Technology of China Siping Gao, Nanjing University of Aeronautics and Astronautics
INVITED TALK	**Advanced Discontinuous Galerkin Method for the Multiphysics Computation of High-Power Microwave Waveguides** *Ping Li, University of Electronic Science and Technology of China* **Power Delivery of Chiplets: Challenges and Opportunities** *Siping Gao, Nanjing University of Aeronautics and Astronautics* **Machine Learning Assisted SI/PI Modeling and Optimization** *Ling Zhang, Zhejiang University* **Innovative PDN Design Using Equivalent Circuits for Enhanced Power Integrity Beyond Decoupling Capacitors** *Zhifei Xu, DeTooLIC Technology*

TITLE	**Advanced Discontinuous Galerkin Method for the Multiphysics Computation of High-Power Microwave Waveguides**
TIME	08:40-09:10 November 7th
VENUE	YuanShi Function Room @Level 2（2楼院士厅）
SPEAKER	Ping Li, University of Electronic Science and Technology of China

ABSTRACT

To comprehensively study the electrical performance of microwave waveguides, an efficient multiphysics computational algorithm based on a Robin Transmission Condition enhanced discontinuous Galerkin (RTC-DG) method is developed to investigate the mutual influences of electromagnetics, thermal and stress in the waveguides. With the proposed RTC-DG algorithm, the high-order PDEs are allowed to be discretized straightforwardly. In addition, to get the surface unknowns in the numerical flux solved, suitable RTCs are developed in terms of the field continuity conditions across the interfaces of neighboring subdomains. As a result, the number of DoFs are remarkably reduced compared with the classic DG method. Furthermore, the impedance boundary condition is exploited to model the metal conductors of the waveguides, and a corresponding equivalent surface heat source is derived in terms of the skin effect, which thus avoids volumetric meshes. In addition, to avoid solving a globally coupled matrix system, the FETI-like strategy is resorted to, which tears the global matrix system into a number of small matrix systems pertinent to each subdomain. Thereby, a direct solver can be deployed to solve these small matrix equations in a parallel way without worrying about the convergence issue. Representative numerical examples will be presented during the conference.

BIOGRAPHY

Dr. Li Ping (Senior Member of IEEE) obtained his Ph.D. from the University of Hong Kong in 2014. He was selected for the Overseas High-level Talent Youth Project in 2018 and is currently a professor in the “Electromagnetic Radiation and Scattering Team” at the University of Electronic Science and Technology of China. From October 2014 to July 2019, he held postdoctoral researcher, research scientist, and assistant professor positions at Purdue University, King Abdullah University of Science and Technology, and the University of Hong Kong, respectively. He has published over 100 papers, including more than 40 papers in IEEE journals. His research achievements have been recognized with several awards at international conferences, including the YITP Award at the IEEE SPI International Symposium in May 2017, the Outstanding Young Scientist Award at the Joint IEEE EMC & APEMC International Conference in May 2018, the Young Scientist Award at the ACES International Conference in July 2018, and the Young Scientist Award

at the PIERS International Conference in August 2018. Additionally, he received the Second Prize in Natural Science from the China Institute of Electronics in 2019, the Okawa Foundation Research Grant Award in 2020, and the China Electronics Society's Innovation Team Award in Electronic Information Technology in 2023.

TITLE	**Power Delivery of Chiplets: Challenges and Opportunities**
TIME	09:10-09:40 November 7th
VENUE	YuanShi Function Room @Level 2（2楼院士厅）
SPEAKER	Siping Gao, Nanjing University of Aeronautics and Astronautics

ABSTRACT

As semiconductor design continues to evolve, chiplet technology has emerged as a promising solution to the limitations of traditional monolithic integrated circuits. The shift towards chiplet-based architectures offers flexibility, scalability, and improved manufacturing yields. However, this new approach presents significant challenges in power delivery. Efficient power delivery in chiplet systems is crucial to maintaining performance and reliability across multiple, independently manufactured and assembled die. In this paper, we explore the key issues surrounding power delivery in chiplet architectures, including power integrity, voltage regulation, interconnect design, and thermal management. We also propose innovative power delivery network (PDN) strategies tailored to the specific needs of chiplet designs. Our findings demonstrate how advanced PDN designs can mitigate power-related issues while supporting the energy efficiency, performance, and scalability demands of future semiconductor systems. This talk provides valuable insights for industry professionals and academics aiming to address the power delivery challenges inherent in the next generation of chiplet-based technologies.

BIOGRAPHY

Si-Ping Gao was a Senior Engineer of AMD. He is currently a Full Professor with NUAA and an Adjunct Assistant Professor with NUS. He has authored more than 100 refereed papers and one book chapter. He holds several patents. His research interests include EMC/EMI, signal and power integrity for 2.5D/3D ICs, RFIC and microwave measurement.

Dr. Gao received the Young Professional Award from the IEEE EMC Society in 2021 and many other technical awards including the APEMC 2016 Best Symposium Paper Award, the SPI 2017 Young Investigator Training Program Award, the URSI GASS 2017 Young Scientist Award, the Outstanding Young Scientist Award at the 2018 Joint IEEE EMC & APEMC Symposium, and the IEEE MTT-S IMWS-AMP 2020 Best Paper Award. He served as the TPC Co-chair of IEEE MTT-S IMWS-AMP 2021, the Technical Paper Chair of APEMC 2022, the Finance Co-Chair of the 2018 Joint IEEE EMC & APEMC Symposium and many other roles at international conferences. He was a Distinguished Reviewer of IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY (2023).

TITLE	**Machine Learning Assisted SI/PI Modeling and Optimization**
TIME	09:40-10:10 November 7th
VENUE	YuanShi Function Room @Level 2（2 楼院士厅）
SPEAKER	Ling Zhang, Zhejiang University

ABSTRACT

With the continuous increase of operating frequency and decrease of power supply voltage in modern integrated circuits (ICs), the signal integrity (SI) and power integrity (PI) design is becoming more and more critical. However, as the design complexity increases, the electronic design automation (EDA) algorithms that can significantly accelerate SI/PI design are urgently demanded. This talk will mainly discuss several recently developed machine-learning techniques for SI/PI design optimization, which have demonstrated great potential to outperform human experience. The design scenarios include decoupling capacitor (decap) optimization for power distribution networks (PDNs), pinmap optimization for electromagnetic interference (EMI) mitigation and SI/PI co-optimization, and design parameter optimization for high-speed interconnects. Further, the challenges and opportunities in this research direction will be discussed.

BIOGRAPHY

Dr. Ling Zhang received the B.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2015, and the M.S. and Ph.D. degrees in electrical engineering from Missouri S&T, Rolla, MO, USA, in 2017 and 2021, respectively. He was with Cisco, San Jose, USA as a Hardware Engineer, from August 2016 to August 2017. He joined Zhejiang University, Hangzhou, China, as a Post-Doctoral Research Fellow, in 2021. He is currently a ZJU100 Young Professor at Zhejiang University. His research interests include machine learning, power integrity (PI), electromagnetic interference (EMI), radio frequency interference (RFI), and signal integrity (SI). Dr. Zhang was a recipient of the Best SIPI Paper Honorable Mention Award in EMC Symposium 2023, the Best Student Paper Award in 2023 International Conference on Microwave and Millimeter Wave Technology, the Honorable Mention Paper in APEMC 2022, the Best Paper Award in DesignCon 2019, the Young Scientist Reward in APEMC 2022, and the 2024 IEEE EMC Society Herbert K. Mertel Young Professional Award.

TITLE	**Innovative PDN Design Using Equivalent Circuits for Enhanced Power Integrity Beyond Decoupling Capacitors**
TIME	10:10-10:40 November 7th
VENUE	YuanShi Function Room @Level 2（2 楼院士厅）
SPEAKER	Zhifei Xu, DeTooLIC Technology

ABSTRACT

As the supply voltages are getting lower while current demands are getting higher, the design of the power delivery network (PDN) becomes very important. To ensure good PDN design, engineers use a large number of decoupling capacitors to ensure power integrity, however, they are limited by the area of the PCB and price of decaps. Therefore, analyze and optimize the current loop path is the best solution to solve the limitations. This workshop will present a new idea for PDN optimization based on extracted equivalent circuit from PDN S-parameters, this extracted equivalent circuit can not only be used as a full-path PDN time-domain transient simulation, but also provides a new way of thinking, evaluating and optimizing the impedance of the PDN. It gives us the opportunity to analyze and optimize your PDN inductance starting from the port inductance representing your PDN structure performance limit without decoupling capacitors.

BIOGRAPHY

Zhifei Xu is the Director of High-Speed Department in DeTool Technology, a fast-growing company in EDA industry. He received the Ph.D. degree in electrical engineering from the Rouen University, France, in 2019. He was a Post-Doctoral Researcher with the Electromagnetic Compatibility (EMC) Laboratory, Missouri University of Science and Technology, USA from 2019-2020. His research areas cover hardware security, signal/power integrity, and EMC analysis in high-speed interconnect systems. His main research direction is the technological breakthrough of EDA tool development in the direction of high-speed signal power supply and electromagnetic field. He has published more than 40 papers on SI/Pl, given academic reports at many international conferences, and published a book on the application of tensor analysis method to EDA design of integrated circuits.

OVERVIEW OF SESSIONS III

SESSIONS	ESD Techniques for Integrated Circuits and Electronic Systems
VENUE	Room 3: JuXian Function Room @Level 2（2 楼聚贤厅）
TIME	8:40-11:30 November 7th
SESSION CHAIR	Shurong Dong, Zhejiang University Fayu Wan, Nanjing University of Information Science and Technology
INVITED TALK	**High-voltage, High-impact ESD Protection Design(高压、高抗扰 ESD 防护设计)** *Dawei Lai, Weixin Technology (Xuzhou) Co., Ltd* **The ESD and EOS Integrated Protection on Chip for Improving the IC Reliability** *Hailian Liang, Jiangnan University* **Investigation on Fabrication-induced High-leakage Issue of an Overdrive ESD Power Clamp in Advanced FinFET Technology** *Guangyi Lu, Southeast University* **Cable Discharge Event Evaluation Methods Discussion** *Bingsheng Gao, ESDEMC Technology* **Research on ESD Protection Technology for RF SOI MOS RF Switch Array** *Shurong Dong, Zhejiang University*

TITLE	**High-voltage, High-impact ESD Protection Design(高压、高抗扰 ESD 防护设计)**
TIME	08:40-09:10 November 7th
VENUE	JuXian Function Room @Level 2（2 楼聚贤厅）
SPEAKER	Dawei Lai, Weixin Technology (Xuzhou) Co., Ltd

ABSTRACT

中国刚刚进入集成电路的性能好而且可靠性要高的过程！在与国外集成电路产品的市场竞争中，可靠性问题是国产集成电路产品的短板，尤其是在高稳定性和可靠性的芯片方面，国内和国外的差距是巨大的。所以我们必须提高并填补国产集成电路和芯片的可靠性短板。而静电放电所产生的破坏又是可靠性里面的一个重要的环节。这次的课题主要分享静电保护的技术挑战，市场需求及如何设计高可靠性的芯片级 ESD 防护。以深入浅出的方式讲解 ESD 防护设计概念，全方面的讲解高压 ESD 设计。最后带领各位探索并且延伸至全芯片 ESD 防护。此课程兼顾理论及配合实例，带领各位一步步了解如何设计高可靠性的 ESD 防护。

BIOGRAPHY

赖大伟于中国台湾交通大学电子专业硕士毕业。有 15 年以上海外知名半导体企业任职经验， 2003 年加入台积电任职 IO ESD 电路工程师；2010 年加入新加坡 GlobalFoundries 任职 ESD 技术经理；2013 年至 2021 年加入荷兰 NXP 公司，任职 IO ESD 首席架构设计师并于 2019 年获得 NXP 著名发明家奖项。现任伟芯科技（徐州）特聘专家、苏州智聚芯联特聘高级顾问、杭州昕未科技特聘高级顾问、西安电子科大企业导师。2024 年评定杭州市西湖明珠人才。

赖大伟长期致力于 IC 领域中的 IO/ESD 保护模块设计，在多家国际头部公司担任核心职位，其技术涵盖 CMOS、SOI 和 HV（高压） BCD 等多种工艺，从 0.18um 到 16nm 线宽均具有丰富的经验。有丰富的车载 ESD 的设计经验，在 NXP 工作期间，负责 40nm 和 16nm 先进工艺的片上 ESD 保护架构设计，解决车载以太网芯片系统级保护难题，单颗芯片降本约 30%，广泛用于其他工艺和产品。并于 2017 年被“EOS/ESD Symposium”授予“Industry Contribution Award”

在个人创新研发方面，赖大伟同志已申请并获得 87 项专利，这些专利经常被业界广泛引用和应用。此外，还在 IEEE 等国际权威期刊上发表了多篇科技论文，这些论文在相关学科领域引起了重大话题和广泛的讨论，并获得较高的学术评价。

TITLE	**The ESD and EOS Integrated Protection on Chip for Improving the IC Reliability**
TIME	09:10-09:40 November 7th
VENUE	JuXian Function Room @Level 2（2 楼聚贤厅）
SPEAKER	Hailian Liang, Jiangnan University

ABSTRACT

围绕智能驾驶、无人机等新兴领域的高可靠 ESD/EOS 防护需求，在当前国产芯片 ESD/EOS 防护面临着严峻技术挑战情势下，本报告主要推介课题组在提升集成电路芯片可靠性研究相关研究进展和成果。重点在提升抗闩锁能力、抑制寄生电容、增强钳位性能、减少芯片面积等方面分享研发案例，阐述课题组在 ESD/EOS 一体化防护中的一些新理念与电路创新方法，分享近期 ESD/EOS 一体化防护研究中经验体会。内容涵盖低压、中压和高压多电源域的 ESD/EOS 一体化防护应用。结合相关仿真模拟与测试分析，解析影响 ESD/EOS 防护性能的集成电路工艺和电路结构等主要制约因素，与同行深入探讨提升电子系统 ESD/EOS 防护等可靠性能的最佳设计方案。

BIOGRAPHY

Dr. Hailian Liang has been engaging the research of ESD and EOS protection over a dozen years. She focus on studying the reliability of integrated circuits, possessing fruitful experience in the design and development of chip electrostatic and surge protection, as well as a good understanding of the electrical performance measurement of different types of electronic systems for electrostatic and surge protection. She firstly developed and verified a high-integrated electrostatic and surge protection method in China, for meeting requirements of on-chip electrostatic protection and port surge protection in electronic systems. She also developed a variety of high-voltage, medium-voltage, and low-voltage anti-latching robust electrostatic and surge protection chips. She served as the main investigator for national and provincial natural science foundation projects, as well as corporation with the enterprise R&D project. In this Seminar, she will share some share some design methods, design cases and experimental lessons of the ESD and EOS integrated protection.

TITLE	**Investigation on Fabrication-induced High-leakage Issue of an Overdrive ESD Power Clamp in Advanced FinFET Technology**
TIME	09:40-10:10 November 7th
VENUE	JuXian Function Room @Level 2（2 楼聚贤厅）
SPEAKER	Guangyi Lu, Southeast University

ABSTRACT

Fabrication-induced high-leakage issue of an overdrive ESD power clamp is presented. With silicon data exhibiting abnormal results, elaborate troubleshooting is performed and disclosed in this paper. Through alignments of silicon data and presumptive simulation results, fabrication-induced root cause is successfully revealed and confirmed by physical failure analysis (PFA) results.

BIOGRAPHY

Guangyi Lu received his B.S., M.S. and Ph.D degrees from Peking University in 2011, 2014 and 2018, respectively. He served as a principal engineer at Hisilicon Technologies from August 2018 to July 2024. He is currently an associate professor with School of Integrated Circuits, Southeast University.

TITLE	**Cable Discharge Event Evaluation Methods Discussion**
TIME	10:10-10:40 November 7th
VENUE	JuXian Function Room @Level 2（2 楼聚贤厅）
SPEAKER	Bingsheng Gao, ESDEMC Technology

ABSTRACT

Cable Discharge Events (CDE) are a significant concern in electronic systems, as they can lead to severe damage in sensitive components and affect overall system reliability. This presentation will provide a comprehensive overview of CDE, including an explanation of what constitutes a CDE, the typical causes behind these events, the potential impacts of CDEs on electronic devices, which may range from temporary malfunction to permanent failure, and the discharge sequence.

Additionally, the presentation will cover our recommended methodologies for evaluating and testing CDE susceptibility in electronic systems. We will introduce two approaches: first, using an TLP generator that mimics typical cable discharge conditions; and second, implementing a CDE test setup that simulates real-world discharge events with high accuracy. These methods provide reliable and repeatable testing conditions that can help identify vulnerabilities and improve design resilience.

Through this presentation, attendees will gain valuable insights into the nature of CDEs and practical strategies for mitigating their effects in electronic designs.

BIOGRAPHY

Bingsheng Gao received his MSc of Physical electronics, specializing in ESD and EMC, from the School of Information Engineering, Wuhan University of Technology. He is currently working as a applications engineer at ESDEMC Technology Co., Beijing Branch. Over the years, he has been mainly engaged in device level and system level ESD and EMC test research, as well as technical support for such test equipment.

TITLE	**Research on ESD Protection Technology for RF SOI MOS RF Switch Array**
TIME	11:00-11:30 November 7th
VENUE	JuXian Function Room @Level 2（2 楼聚贤厅）
SPEAKER	Shurong Dong, Zhejiang University

ABSTRACT

RF switches are widely used in mobile communication fields such as mobile phones, Bluetooth, WIFI, and satellite communication. As the backend of the antenna directly connected to the chip, they are often damaged or soft fail due to ESD impact. The ESD protection technology of RF SOI MOS RF switche array is researched in this paper. Three main ESD failure problems of this chip is investigated including ESD risk window by power on, secondary ESD zipping from system, and RCNMOS protection system effectiveness. Their failure mechanisms are provide by failure analysis and modeling simulation verification, and circuit optimization are carried out. The improvement and design rule of ESD protection are given, which has been applied in Vanchip produces.

BIOGRAPHY

Shurong Dong received his PHD of Electronic Engineering from the ISEE College of Zhejiang University. He is currently working as a Professor of ISEE College of Zhejiang University. Over the years, he has been mainly engaged in device level and system level ESD and EMC research.

OVERVIEW OF SESSIONS IV

SESSIONS	EMC Techniques for Integrated Circuits
VENUE	Room 1: JiangNan Function Room @Level 2（2 楼江南厅）
TIME	13:30-17:20 November 7th
SESSION CHAIR	Qiang Cui, China Electronics Standardization Association Jianfei Wu, Tianjin Institute of Advanced Technology
INVITED TALK	**Thoughts on Forward Design Technology for Electromagnetic Compatibility and Protection of Chips/Boards** *Zhaowen Yan, Beihang University* **Research and Practical Cases on Electromagnetic Compatibility Testing Technology for Automotive Chips (车规芯片电磁兼容测试技术研究及实际案例)** *Qiang Cui, China Electronics Standardization Association* **Near Field Scanning Techniques for IC** *Wenxiao Fang, Sun Yat-sen University* **Multi-physical Field Coupling Characteristics of IC Pins Distribution on High-frequency Flexible PCB** *Mengjun Wang, Hebei University of Technology* **Study on Electrostatic Discharge Sensitivity of Integrated Circuits** *Xiaojun Hu, 3C Test* **Mechanism of Multi-physical Field Effects in RF CMOS Circuits and MEMS Devices** *Shitao Chen, Anhui University*

TITLE	**Thoughts on Forward Design Technology for Electromagnetic Compatibility and Protection of Chips/Boards**
TIME	13:30-14:00 November 7th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Zhaowen Yan, Beihang University

ABSTRACT

This report focuses on the electromagnetic safety issues faced by domestic chips in complex electromagnetic environments, and explores the importance of accurately obtaining the electromagnetic boundaries of chips and achieving forward design. The report introduces the precise detection technology of chip electromagnetic emission, electromagnetic sensitivity, and electromagnetic vulnerability. It also introduces the modeling methods of chip conduction emission, near-field radiation emission, conduction sensitivity, and electromagnetic vulnerability. The report will also explore the forward design methods for chip level and board level electromagnetic compatibility and protection based on the chip electromagnetic compatibility model in the product development process.

BIOGRAPHY

Zhaowen Yan received the B.S. degree, the M.S. degree and the Ph.D degree in electrical engineering from Henan Polytechnic University, Xi'an University of Science and Technology and Xi'an Jiaotong University, China, in 1991, 1996 and 1999, respectively. From 1999 to 2002 he was a Post-Doctoral Research Associate at the Huazhong University of Science and Technology. From April 2003 to May 2005, he hold a Post-Doctorial position at Beihang University. From December 2012 to December 2013, he is a visiting scholar in EMC Laboratory, Missouri University of Science and Technology, U.S.A.

He is now a professor of electronic science and technology at Beihang University. For many years, his research activity was focused on the electromagnetic field computation and EMC analysis. He has published over 150 conferences and journal papers and 8 monographs on electromagnetic theory. He has 41 authorized patents. He won the first prize of the Natural Science of the Ministry of Education of PRC in 2003 and the first prize of National Defense Science and Technology Progress in 2011 as recognition of his research work. And the project he held won the second prize for the National Science and Technology Progress in 2012. He also won the first prize for National Defense Technology Invention in 2017. He won the first prize of the National Technology Invention in 2018.

TITLE	**Research and Practical Cases on Electromagnetic Compatibility Testing Technology for Automotive Chips (车规芯片电磁兼容测试技术研究及实际案例)**
TIME	14:00-14:30 November 7th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Qiang Cui, China Electronics Standardization Association

ABSTRACT

解读国家标准车规芯片电磁兼容标准主要技术内容，研究该标准中给出的测试项目和测试方法，分享车规芯片的实际测试经验。

BIOGRAPHY

崔强，博士，长期从事电磁兼容课题研究、标准制定和检测，现任电磁环境效应标准化技术委员会秘书、全国无线电干扰标准化技术委员会 A 分会秘书长、集成电路电磁兼容标准工作组组长等。作为主要起草人，主办/参加了 60 多项国家和行业电磁兼容标准的制修订工作，在各类会议及期刊上发表技术论文 20 多篇，完成了多项部级课题的研究工作，获得省部级奖 6 项，著译作 6 部。

TITLE	**Near Field Scanning Techniques for IC**
TIME	14:30-15:00 November 7th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Wenxiao Fang, Sun Yat-sen University

ABSTRACT

In this talk, the near field scanning techniques for IC is presented. The background for near field scanning techniques is introduced. Then principle of the near field probe and how it is designed are both explained with details. Based on the probes, the scanning techniques for IC is also introduced with the post process, such as pattern extraction, grouping, and denoise method of the scanning data. And finally, we also share the understanding of the emission pattern of IC, and the phase effect inside the emission pattern.

BIOGRAPHY

Wenxiao Fang received the B.S., M.S., and Ph.D. degrees in condensed-matter physics from Sun Yat-sen University, Guangzhou, China, in 2002, 2005, and 2008, respectively. He was a Visiting Scholar with Hong Kong University of Science and Technology, Hong Kong, in 2009. After that, he joined China Electronic Produce Reliability and Environmental Testing Research Institute and severed as a Senior Engineer of the science and technology on reliability physics from 2011. In 2023, he joined the school of IC in Sun Yat-sen University and serve as a professor. His current interests include the electromagnetic compatibility in integrated circuit and component level and electromagnetism application in power electronics

TITLE	**Multi-physical Field Coupling Characteristics of IC Pins Distribution on High-frequency Flexible PCB**
TIME	15:00-15:30 November 7th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Mengjun Wang, Hebei University of Technology

ABSTRACT
In order to study the reliability of the internal interconnect structure of flexible electronic devices under the load of high-frequency signals, the electromagnetic, temperature, and mechanical characteristics of IC pins on flexible PCB from 0.45 GHz to 15 GHz are investigated. By simulating the overall failure of the flexible electronic devices under the combined influence of the device power dissipation and the conductor loss generated by the high-frequency electrical signals through the interconnect pins. The effects of different pitch and distance from the chip on the reliability of the flexible electronic device are also analyzed for the pins flowing through the high-frequency signals. The simulation results show that the smaller the pitch of the interconnect pins and the closer the distance to the chip, the higher the temperature and the higher the stress. Furthermore, this trend becomes more pronounced as the operating frequency increases. This study provides ideas for optimizing the effectiveness of thermal management and the structural reliability of the entire flexible electronic device.

BIOGRAPHY
Mengjun Wang was born in Hebei, China, in 1978. He received his B.S. degree in information engineering and M.S. degree in physical electronics from Hebei University of Technology, Tianjin China, in 1999 and 2005, respectively, and Ph.D. degree from Tianjin University, Tianjin, China, in 2008.
He is working as an associate professor at School of Electronics and Information Engineering, Hebei University of Technology, Tianjin, China. His research interests include microwave radio frequency technology, flexible electronics devices and electromagnetic compatibility. He is also working as a member of the First Electromagnetic Compatibility Risk Assessment Committee (SAC/TC227/SC6) of the National Radio Interference Standardization Technical Committee, member of TC599 Integrated Circuit Electromagnetic Compatibility Standardization Working Group of the Ministry of Industry and Information Technology of China.

TITLE	**Study on Electrostatic Discharge Sensitivity of Integrated Circuits**
TIME	15:30-16:00 November 7th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Xiaojun Hu, 3C Test

ABSTRACT
One of the important factors causing potential or fatal failures in silicon chips is electrostatic discharge (ESD). We are familiar with ESD models and evaluation methods, including the human body model (HBM), machine model (MM), and charging model (CDM), which directly simulate certain types of static electricity in the real world. The transmission line pulse model is different from the above models and does not simulate real-world static electricity. Instead, it uses nanosecond-level square wave pulses to obtain the impedance characteristics of the chip (I-V curve) and reveal its electrostatic protection characteristics.

BIOGRAPHY
Currently serving as the Director of Standard Regulation Research Department and Manager of Product Department at Suzhou Taisite Electronic Technology Co., Ltd., Mr. Hu has over 20 years of experience in EMC testing and practical application. He also serves as a member of the Sub-Technical Committee on Measurement Methods and Statistical Methods of Radio Interference of the National Technical Committee on Electromagnetic Compatibility (A Sub-Committee), a member of the Sub-Technical Committee on High-Frequency Phenomena of the National Technical Committee on Electromagnetic Compatibility (B Sub-Committee), a correspondent member of the Sub-Technical Committee on Radio Interference of Mobile Vehicles and Internal Combustion Engines of the National Technical Committee on Electromagnetic Compatibility (D Sub-Committee), and a member of the EMC Working Group on Integrated Circuits

TITLE	**Mechanism of Multi-physical Field Effects in RF CMOS Circuits and MEMS Devices**
TIME	16:20-16:50 November 7th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Shitao Chen, Anhui University

ABSTRACT

The development of the Internet of Everything and intelligent industrialization has brought new development opportunities for the high-density heterogeneous integration of RF integrated circuits and MEMS micro-nano structured devices. It isn't easy to build modeling and engineering EDA that approximates the physical reality, but it is crucial for developing high-quality processes and the performance of chips. The high-density heterogeneous integration of multiple physical field force-electromagnetic-heat inside RF systems is often a weak coupling effect. This report will take the multi-physical field-strength coupling interaction model of specific devices as an example to discuss the electromagnetic field-circuit coordination technology of active circuits in microwave integrated circuits, the electro-thermal coupling effect of semiconductor devices, and the force-electromagnetic thermal coupling effect of FBAR filters in new devices. The multi-field coupling problem of force-electromagnetic-thermal and acoustic damping fields of optical MOEMS micro nanostructure with higher operating frequency is also discussed. The speaker puts forward some key techniques in EDA multi-physics simulation to solve the problem of high-density heterogeneous integration of multiple physics fields.

BIOGRAPHY

Chen Shitao is an associate professor and master's degree supervisor at the School of Electronic Information Engineering, at Anhui University. A member of the Communist Party of China and a returned overseas talent in Anhui Province/a high-level talent in Hefei. Focusing on the basic scientific research of national integrated chips and the development needs of provincial and municipal chip industries, he engages in research on RF CMOS integrated circuit chips, MEMS integrated device chips, and artificial intelligence technology. In the past five years, he has presided over projects such as the National Natural Science Foundation for Young Scientists, the Anhui Province University Collaborative Innovation Project, the Anhui Province Postdoctoral Science Foundation Support Project, the Ministry of Industry and Information Technology Key Laboratory Development Project on "Electromagnetic Simulation and RF Perception" at Nanjing University of Science and Technology, and technical research and development projects on chip technology at Suzhou Han Tianxia Electronics Co., Ltd. and the East China Photoelectric Integrated Device Research Institute. He has published more than 10 academic papers as the first author/corresponding author in journals such as TMTT, AWPL, and MWCL, among which 5 are in the second zone of the Chinese Academy of Sciences or above; he has applied for more than 10 Chinese invention patents as the first inventor.

OVERVIEW OF SESSIONS V

SESSIONS	Advanced EMI Modelling and Measurement Technologies
VENUE	Room 2: YuanShi Function Room @Level 2（2 楼院士厅）
TIME	13:30-17:20 November 7th
SESSION CHAIR	Xing-Chang Wei, Zhejiang University Da Yi, Chongqing University
INVITED TALK	**Failure Mechanism and Electromagnetic Compatibility Design of Digital Control Circuit in Mixed Electromagnetic Environment** *Henglin Chen, Zhejiang University* **A Method of Analyzing the Impact of the Wiring Parameters on the Electromagnetic Coupling to PCB Inside Electronic Equipment** *Pei Xiao, Hunan University* **EMI Simulation and Analysis Between Active Chips within Shared Shielding Can** *Da Yi, Chongqing University* **A Convolutional Neural Network-Based Method for Modeling Electromagnetic Interferenced Image Sensor** *Qibo He, OPPO* **Research on the Principles and Applications of Filtering Cables for Protection in Complex Electromagnetic Environments** *Yunan Han, Beijing University of Chemical Technology* **Evaluation of Non-linear Characteristic of Magnetic Core for Compact EMI Filter Design** *Anfeng Huang, DeTooLIC Technology* **Electromagnetic Compatibility Issues of Neuromorphic Chips and Heterogeneous Integrated Circuits** *Yan Li, China Jiliang University*

TITLE	**Failure Mechanism and Electromagnetic Compatibility Design of Digital Control Circuit in Mixed Electromagnetic Environment**
TIME	13:30-14:00 November 7th
VENUE	YuanShi Function Room @Level 2（2 楼院士厅）
SPEAKER	Henglin Chen, Zhejiang University

ABSTRACT

This report deals with failure problem of digital control circuit working in a mixed electromagnetic environment. The digital circuit failure behaviors under mixed electromagnetic interference of electrical fast transient (EFT) and surge are tested and analyzed. The Pearson correlation coefficient algorithm is used to calculate the correlation coefficient between the voltage waveform characteristic parameters of the regulator chip power supply port and the failure behavior. Combined with the test results, it is found that the instantaneous product of amplitude and slope of the power supply port voltage of the regulator chip is the key factor causing the failure of the digital control circuit. Then, a failure threshold evaluation method and a failure prediction model of the digital control circuit are established. Furthermore, an anti-interference filter design

method is presented. The failure threshold evaluation method presented in this report can be applied to evaluating the failure state of digital circuits in the case where both voltage and current may change under mixed electromagnetic interference.

BIOGRAPHY

Henglin Chen was born in Ji'an, Jiangxi, China, in 1979. He received the Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2007.

Since 2008, he has been with the College of Electrical Engineering, Zhejiang University, where he was a Postdoctoral Researcher between January 2008 and September 2009, and was a Lecturer between October 2009 and December 2011. He was promoted as an Associate Professor in December 2011. From May 2011 to May 2012, he was a Visiting Scholar in Clemson University, Clemson, SC, USA. He has published one book on fundamentals of EMC design for power electronic systems and authored more than 90 papers on EMC technology and theory. His main research interests include power electronics and electromagnetic compatibility.

Dr. Chen was the recipient of the Young Scientist Award from IEEE Asia-Pacific Electromagnetic Compatibility in 2016, and the Best Paper Award from the 13th IEEE Vehicle Power and Propulsion Conference in 2016. He was a General Chair for the 2024 China Power Supply Society EMC Conference, a Chair for the Smart Grid and Low Frequency EMC in the 2022 APEMC, a Chair for the Topical Symposium on Smart Grid & Power Electronics EMC in the 2018 Joint IEEE EMC & APEMC, a Session Chair in the 2017 Asia-Pacific Electromagnetic Week Conference on Electromagnetic Compatibility, a Session Chair for the Special Session on EMC Issues in Electric Vehicles in the 2016 IEEE VPPC Conference, and a Chair for the 2016 APEMC Topical Symposium on Smart Grid & Power Electronics EMC.

TITLE	**A Method of Analyzing the Impact of the Wiring Parameters on the Electromagnetic Coupling to PCB Inside Electronic Equipment**
TIME	14:00-14:30 November 7th
VENUE	YuanShi Function Room @Level 2（2 楼院士厅）
SPEAKER	Pei Xiao, Hunan University

ABSTRACT

Interconnection cables, as the carrier of signal and energy transmission in electromechanical equipment, are an indispensable part of realizing system functions. Because of the cables' antenna effect, they provide a main gateway for electromagnetic interference and play a major role in electromagnetic compatibility. This paper introduces an method for designing cable shielded structures, leveraging the power of an artificial neural network algorithm. By utilizing key parameters such as core wire radius, insulation layer radius, and outer insulation layer thickness as training inputs, the algorithm is trained to predict transfer impedance curves as its output. Following the training phase, the artificial neural network demonstrates well accuracy in predicting transfer impedance. This capability allows the proposed method to be seamlessly integrated with optimization algorithms, enabling the tailored design of cable shielded structures to meet specific transfer impedance requirements with precision.

BIOGRAPHY

Born in December 1989, Associate researcher/Assistant professor of Hunan University, backbone of Antenna and Electromagnetic Compatibility Research Center of Hunan University. Research interests include electromagnetic compatibility simulation and design, electromagnetic effects and electromagnetic protection, antenna theory and design, etc. He has published more than 40 high-level papers and journals, authorized 10 international/national invention patents, more than 10 utility model patents, and 5 software works. In recent years, he has presided over more than 10 projects such as the Science and Technology Commission of the Military Commission 173, the National Natural Science Foundation of China, and the Equipment Development Department of the Military Commission.

TITLE	**EMI Simulation and Analysis Between Active Chips within Shared Shielding Can**
TIME	14:30-15:00 November 7th
VENUE	YuanShi Function Room @Level 2（2 楼院士厅）
SPEAKER	Da Yi, Chongqing University

ABSTRACT

This work studies the resonance-dominated-interference between the active chips in a shared shielding can. First, the two passive traces case is considered for reference, and later two power amplifier (PA) chips are integrated for study. A co-simulation method is proposed by combining the multi-port 3-D full-wave simulation and circuit simulation to predict and analyze the complex coupling phenomena between two chips in a shared shielding can. Finally, a novel diaphragm, which is based on the single-negative (SNG) metamaterial, is designed to introduce broadband compartment shielding performance. Experimental results demonstrate the effectiveness of the above simulation method and suppression technique.

BIOGRAPHY

Da Yi received the B.S. and Ph.D. degrees in electronic science and technology from Zhejiang University, Hangzhou, China, in 2014 and 2019, respectively. He is currently a Tenure-Track Assistant Professor with Chongqing University, Chongqing, China. His current research interests include interference decoupling and noise suppression in antenna arrays and high-speed circuits. He was a recipient of awards in several international conferences, including the Best Student Paper Award in IWS 2016 and EMC COMPO 2019, the Best Paper Award in ISEMC 2019, the Young Investigator Training Program Award in SPI 2017, and the Young Scientist Award in APEMC 2022.

TITLE	**A Convolutional Neural Network-Based Method for Modeling Electromagnetic Interferenced Image Sensor**
TIME	15:00-15:30 November 7th
VENUE	YuanShi Function Room @Level 2（2 楼院士厅）
SPEAKER	Qibo He, OPPO

ABSTRACT

EMI (Electromagnetic Interference) on Image sensors may incurred image dark stripes, which is a common and severe problem within highly integrated electronic system such as mobile phones. This paper presents a convolutional neural network (CNN)-based method for accurately modeling the disturbed image sensor for EMI analysis and prediction without accessing the inner circuit design. By importing simulated magnetic field maps into CNN, the trained CNN output the predicted TN(Temporal noise) value, reflecting the interference on sensors under various electromagnetic field environments. This proposed method provides an accurate assessment with average errors under 1, which is efficient and effective for the layout design in electronic products.

BIOGRAPHY

Leader of OPPO Electromagnetic Simulation Group, responsible for building precise simulation testing capabilities such as SIPI, low-frequency magnetic interference, board level interference, ESD simulation, etc. By focusing on the miniaturization and slimness of mobile phones, OPPO has achieved multiple breakthroughs in simulation technology, effectively solving many product problems and leading the industry in electromagnetic simulation applications. At the same time, we have conducted in-depth research on multi physics field coupling and the application of AI technology in simulation. In the future, we will continue to carry out new technology research and expand applications around product requirements in related fields.

TITLE	**Research on the Principles and Applications of Filtering Cables for Protection in Complex Electromagnetic Environments**
TIME	15:30-16:00 November 7th
VENUE	YuanShi Function Room @Level 2（2 楼院士厅）
SPEAKER	Yunan Han, Beijing University of Chemical Technology

ABSTRACT

电缆作为工业的血管和神经，需要演进出具有分布式滤波功能的滤波电缆以适应日益复杂的电磁环境。本文提出了一种用于控制电磁干扰（EMI）的滤波电缆，通过将电源线包裹在柔性印刷电路板构成的悬置耦合电路（CSC）中实现滤波功能。该悬置耦合电路由缺陷导体层（DCL）和表面贴电容组成。针对滤波电缆建立了等效电路模型，该模型的构建通过仿真缺陷导体层上的电流分布，进一步等效成对应的微带滤波器的电流分布，提取其不连续模块的电路模型。该滤波电缆在 21.49 MHz 时达到超过 11 dB 的干扰抑制，对于单个哑铃形缺陷结构（35 mm 长度，传输介质直径为 24.3 mm）的电容为 1.36 nF，在 39.52 MHz 时达到 15.8 dB，电容为 400 pF。此外，对于 600 mm 长度的哑铃形缺陷结构和电容为 9.82 nF，所提出的滤波电缆在单个谐振器时实现了超过 5.98 dB 的干扰抑制，而在两个级联谐振器时在 2.27 MHz 时达到了 9.26 dB。仿真和测试结果表明，所提出的滤波电缆实现了有效的 EMI 抑制，实际应用中可以通过修改哑铃形缺陷结构的面积、电容器以及谐振器的级联来进一步调整其滤波性能。与传统电缆相比，这种滤波电缆通过切断干扰耦合路径来解决电磁兼容性问题，在信息和智能化时代有非常可观的应用前景。

BIOGRAPHY

韩宇南，北京化工大学副教授，硕士生导师。2007 年获北京邮电大学电磁场与微波技术专业博士学位。研究方向为系统电磁兼容、强电磁脉冲防护、静电放电、天线设计等，是滤波电缆国际专利的发明人。2007-2010 年在中国航天集团第一研究院第一设计部从事多个重点型号的电磁兼容设计，2013.3-2014.3 在美国密苏里科技大学电磁兼容实验室做访问学者。 发表论文 50 余篇，授权发明专利 20 余项。主持国家自然科学基金面上项目，北京市自然科学基金面上项目，多项军工项目。

TITLE	**Evaluation of Non-linear Characteristic of Magnetic Core for Compact EMI Filter Design**
TIME	16:20-16:50 November 7th
VENUE	YuanShi Function Room @Level 2（2 楼院士厅）
SPEAKER	Anfeng Huang, DeTooLIC Technology

ABSTRACT

Electromagnetic interference (EMI) remains a constant challenge in modern electronic devices, requiring strict adherence to EMI regulations for market clearance. As a result, tackling EMI has become a major obstacle for power electronics designers. Conventional passive EMI filters frequently occupy a substantial portion of the volume in power electronics systems. Furthermore, the size bottleneck lies in the magnetic core's volume, which remains large to avoid saturation caused by significant common-mode currents. In this presentation, we showcase an evaluation method for assessing the impedance of chokes under AC saturation conditions. Additionally, we introduce an Active EMI Filter IC as a solution to reduce the bulkiness of traditional passive EMI filters.

BIOGRAPHY

Anfeng Huang (Member, IEEE) received the B.E. and M.S. degrees in electrical engineering from Xidian University, Shaanxi, China, in 2014 and 2017, respectively, and the Ph.D. degree in electrical engineering from the Missouri University of Science and Technology, Rolla, MO, USA, in 2022. He is currently with Detooltech, Ningbo, China. His current research interests include EMI in power electronics, magnetic material characterization, and advanced measurement techniques.

TITLE	**Electromagnetic Compatibility Issues of Neuromorphic Chips and Heterogeneous Integrated Circuits**
TIME	16:50-17:20 November 7th
VENUE	YuanShi Function Room @Level 2（2楼院士厅）
SPEAKER	Yan Li, China Jiliang University

ABSTRACT

With the rapid advancement of artificial intelligence technology, intelligent chips and their heterogeneous integrated circuits (HIC) have found extensive applications in high-performance computing, autonomous driving, 5G communications, the Internet of Things (IoT), and other fields. However, the diversity and complexity of heterogeneous integration architectures present significant electromagnetic compatibility (EMC) challenges during their design and implementation. This report delves into the EMC issues encountered in intelligent chips and heterogeneous integrated circuits, analyzing the underlying causes and influencing factors, and proposes optimized designs and solutions tailored to various application scenarios. Key topics include electromagnetic interference analysis of intelligent chips in high-frequency, broadband, and multimodal environments; electromagnetic coupling issues in heterogeneous integrated circuits under conditions of high integration density and frequency diversity; and cutting-edge research progress in enhancing EMC performance through new materials, structural design, and machine learning algorithm optimization. The report aims to provide researchers and engineers with innovative EMC design perspectives and practical guidance, fostering the development and application of intelligent chip and heterogeneous integrated circuit technologies.

BIOGRAPHY

Dr. Li Yan, a native of Weifang, Shandong Province, is currently a graduate supervisor at the College of Information Engineering, China Jiliang University. She earned her Ph.D. in Electrical Engineering from Hebei University of Technology, with joint training experience at both Zhejiang University and Hebei University of Technology. Dr. Li is a Senior Member of IEEE, a Senior Member of the Chinese Institute of Electronics, and a Senior Member of the Zhejiang Communication Association. Additionally, she serves on the Electromagnetic Compatibility (EMC) Standards Working Group for Integrated Circuits and is a committee member of the Risk Assessment Subtechnical Committee under the National Radio Interference Standardization Technical Committee. Her research primarily focuses on computational electromagnetics, microwave theory and techniques, with specialized expertise in electromagnetic compatibility (EMC/EMI), power and signal integrity of 3D integrated circuits, neuromorphic chips, 5G communication devices, issues in electronic packaging, and the design of electromagnetic shielding structures.

Since 2017, Dr. Li has published over 60 high-impact papers and actively contributes as a reviewer for numerous IEEE journals. She has also served as an organizing committee member or session chair for international academic conferences. Dr. Li has been the principal investigator on multiple national and provincial research projects, including those funded by the National Natural Science Foundation of China and the Zhejiang Provincial Natural Science Foundation, as well as several collaborative projects with industry partners. In recognition of her significant contributions, she was awarded the IEEE EMC Society’s Technical Achievement Award in 2023 and has received multiple honors from the China Invention Association’s Innovation and Entrepreneurship Awards, as well as the IEEE Young Scientist Award. Her cutting-edge research encompasses AI-driven advancements in electromagnetic and signal integrity for neuromorphic chips, establishing her as a leading expert in these forefront technologies.

OVERVIEW OF SESSIONS VI

SESSIONS	Signal/Power Integrity and Multiphysics Analysis for Chiplets
VENUE	Room 3: JuXian Function Room @Level 2（2 楼聚贤厅）
TIME	13:30-17:20 November 7th
SESSION CHAIR	Bo Pu, DeTooLIC Technology Wenchao Chen, Zhejiang University
INVITED TALK	**Machine Learning-Assisted Modeling and Simulation of Chiplet Based High Speed IOs** *Cheng Zhuo, Zhejiang University* **Crosstalk Cancellation Circuit Design Techniques for High-Density and High-Speed Interconnects** *Yuan Du, Nanjing University* **Exploration of Multi-physics Modeling and Intelligent Technologies** *Qiwei Zhan, Zhejiang University* **Multiphysics and Nonlinearity Modeling/Measurement of RF Interconnects** *Wenchao Chen, Zhejiang University* **Exploring EDA Tools for Collaborative Design and Simulation of 2.5D/3D ICs in Advanced Packaging** *Yi Zhao, Zhuhai Silicon Chip Technology Ltd.* **Evolution and Prospect of High-Density Chiplet Integration Technology** *Shujuan Liu, Yangtze Laboratory* **Research on the Reliability of 2.5D/3D IC under Multi Physical Field Coupling** *Jiahao Zhou, DeTooLIC Technology*

TITLE	**Machine Learning-Assisted Modeling and Simulation of Chiplet Based High Speed IOs**
TIME	13:30-14:00 November 7th
VENUE	JuXian Function Room @Level 2（2 楼聚贤厅）
SPEAKER	Cheng Zhuo, Zhejiang University

ABSTRACT
In the post-Moore era, as the limitations of traditional integrated circuit scaling laws become increasingly apparent, chiplet-based heterogeneous integration technology is gradually becoming a new driving force for the development of the semiconductor industry. Traditional circuit modeling and simulation methods struggle to handle the complex interdependencies and massive circuit scales introduced by advanced chiplet architectures. This talk delves into the innovative applications of Machine Learning (ML) in enhancing chiplet circuit modeling and simulation. By incorporating machine learning techniques, complex scenarios can be processed rapidly, simulation time can be shortened, and design iterations can be accelerated. This addresses the challenges posed by the complexity and performance demands of chiplet integrated circuits, improves system integration and performance, and tackles the diverse challenges of heterogeneous integration technology.

BIOGRAPHY
Cheng Zhuo received his Ph.D. from the University of Michigan, Ann Arbor, in 2010. He is currently a Full Professor at Zhejiang University with research focus on hardware intelligence, machine learning-assisted EDA,

and low power designs. He has published over 200 technical papers and received 5 Best Paper Awards, 6 Best Paper Nominations, and 2 international design contest awards. He has served on the organization/technical program committees of many international conferences, as the area editor for Journal of CAD&CG, and as Associate Editor for IEEE TCAD, ACM TODAES, and Elsevier Integration. He is IEEE CEDA Distinguished Lecturer, a senior member of IEEE, and a Fellow of IET.

TITLE	**Crosstalk Cancellation Circuit Design Techniques for High-Density and High-Speed Interconnects**
TIME	14:00-14:30 November 7th
VENUE	JuXian Function Room @Level 2（2 楼聚贤厅）
SPEAKER	Yuan Du, Nanjing University

ABSTRACT

The ever-increasing demand for bandwidth and capacity in data centers and edge high-performance computing devices has driven the continuous development of short-reach, high-speed interconnect technology. In this report, we present a case study of a high-speed transceiver design, specifically tailored for scenarios involving severe crosstalk channels between high-speed, high-density chiplets. The proposed design aims to address the challenges associated with crosstalk cancellation in high-density and high-speed interconnects, enabling the realization of advanced data rates while maintaining signal integrity.

BIOGRAPHY

Yuan Du received his B.S. degree from Southeast University (SEU), Nanjing, China, and his M.S. and Ph.D. both from University of California, Los Angeles (UCLA). He worked for Kneron Inc., San Diego, CA, USA from 2016 to 2019, as a leading hardware architect. Since 2019, he has been with Nanjing University, Nanjing, China, as an Associate Professor. His current research interests include designs of high-speed interconnect transceivers, high-speed inter-chip/intra-chip interconnects, and heterogeneous computing systems.

TITLE	**Exploration of Multi-physics Modeling and Intelligent Technologies**
TIME	14:30-15:00 November 7th
VENUE	JuXian Function Room @Level 2（2 楼聚贤厅）
SPEAKER	Qiwei Zhan, Zhejiang University

ABSTRACT

With the enhancement of computing power, the intersection of numerical simulation and artificial intelligence has formed a new direction----scientific machine learning. The former is featured by the precision of abstract models, while the latter excels in the real-time nature of prediction and inference. However, in the case of complex systems—such as ultra-high-density interconnections, integrated microsystems, and large-scale chip integration—the discrepancies between simulation and observation cannot be ignored. Advanced computing methods, represented by cross-scale computing, multi-physical field modeling, and uncertainty quantification, have emerged in recent years. Currently, intelligent electromagnetic-multi-field modeling is largely limited to simpler scenarios, and the exploration of its incremental capabilities for large-scale practical problems remains necessary. Therefore, it is essential to investigate new artificial intelligence technologies, which transcend the simulation on the data utilization side, striving to achieve true incremental advancement and empowerment.

BIOGRAPHY

Qiwei Zhan received the B.S. degree from the University of Science and Technology of China, Hefei, China, in 2013, the M.S. degree in civil and environmental engineering from Duke University, Durham, NC, USA, in 2016, and the Ph.D. degree in electrical and computer engineering from Duke University, in 2019. From June 2019 to August 2020, he was a Peter O'Donnell, Jr. Postdoctoral Fellow in Oden Institute for Computational Engineering and Sciences, at University of Texas, Austin. Since September 2020, he has been with the College

of Information Science and Electronic Engineering at Zhejiang University as a tenure-track Professor and Ph.D. Supervisor. He is a recipient of the National Science Foundation for Excellent Young Scholars of China. His research interests include multiphysics modeling, computational electromagnetics, computational mechanical waves, uncertainty quantification, effective medium theory, inverse design for metasurface, data assimilation, and scientific machine learning.

TITLE	**Multiphysics and Nonlinearity Modeling/Measurement of RF Interconnects**
TIME	15:00-15:30 November 7th
VENUE	JuXian Function Room @Level 2（2 楼聚贤厅）
SPEAKER	Wenchao Chen, Zhejiang University

ABSTRACT

With the rapid development of wireless communication and satellite communication technologies, the interference caused by passive intermodulation is becoming increasingly significant for communication systems. This talk mainly introduces the Multiphysics modeling and the physical mechanisms of PIM generation by the nonlinearity in metal contact and material. The sources of nonlinearity in contact mainly include the tunneling effect, thermionic emission, etc., and affected by surface roughness, mechanical stress and symmetry of contacts. The nonlinearity in material mainly comes from thermo-electric coupling effect and nonlinear source scattering effect, and affected by geometric structure and point-like stains. In future, it is necessary to go deep into the microscopic field and integrate with Multiphysics modeling technologies to fully reveal the mechanisms of PIM, and then guide the related design of PIM suppression.

BIOGRAPHY

陈文超，浙江大学研究员、博士生导师，浙江大学集成电路学院副院长，国家优青基金、浙江省杰青基金获得者。陈博士针对先进三维集成电路中电磁及多物理效应与可靠性问题，开展了从有源器件/无源器件到电路多层次、多尺度多物理场计算方法与应用研究，已发表论文 100 余篇，他引 3000 余次；曾获 IEEE MTT-S IMWS 2016 国际会议最佳论文奖、PIERS2023 青年科学家奖、中国光学工程学会科技进步二等奖等奖项。

TITLE	**Exploring EDA Tools for Collaborative Design and Simulation of 2.5D/3D ICs in Advanced Packaging**
TIME	15:30-16:00 November 7th
VENUE	JuXian Function Room @Level 2（2 楼聚贤厅）
SPEAKER	Yi Zhao, Zhuhai Silicon Chip Technology Ltd.

ABSTRACT

The adoption of advanced packaging techniques, such as 2.5D Chiplet/3D IC stacked chips, is driving a significant upgrade in the semiconductor industry by addressing design and manufacturing bottlenecks like the memory wall, power wall, and area wall. However, 2.5D Chiplets and 3D ICs present substantial challenges in physical design and simulation verification, creating new demands for next-generation stacked chip EDA tools. These challenges include managing new unit structures like TSVs during the design phase (resulting in a qualitative shift in EDA characteristics compared to traditional tools), a dramatically increased design space due to multi-chip integration and TSVs (leading to a substantial rise in computational complexity), and the heightened difficulty of thermal, electrical, and magnetic multi-physics simulations due to ultra-high-density heterogeneous integration in advanced packaging. This presentation will delve into these challenges and requirements.
Additionally, the presentation will highlight research conducted by Zhuhai Silicon Chip Technology Ltd. on Chiplet-Interposer-Package Co-design and Performance-Cost-Testability Co-optimization. It will also cover

the latest EDA tools for 2.5D/3D ICs, including Chiplet physical design (2.5D layout and routing), multi-physics simulations (SI, PI, thermal analysis), and advanced packaging Chiplet multi-die DFT testing.

BIOGRAPHY

Dr. Yi Zhao, Founder of Zhuhai Silicon Chip Technology Ltd., earned his Ph.D. from the University of Southampton in the UK, under the mentorship of Professor Hashimi, a Fellow of the Royal Academy. Since 2008, Dr. Zhao has been researching 2.5D/3D stacked chip design methods, becoming a key member of one of the earliest research teams worldwide focused on advanced chip architecture. He also collaborated with IMEC on 3D IC validation. With over 15 years of experience in 3D integrated circuit design, he has achieved world-leading results in backend EDA for stacked chips, including layout, routing, testability design, and reliability assurance. His work has been published in top international journals, and he has received the VLSI-SOC International Best Paper Award.

Currently, Dr. Zhao serves as the General Manager and CTO of Zhuhai Silicon Chip Technology Ltd. He leads his team in developing EDA software products for 2.5D Chiplet/3D IC stacked chip design, supporting the advancement and iteration of China's chip design products and promoting domestic self-reliance.

TITLE	**Evolution and Prospect of High-Density Chiplet Integration Technology**
TIME	16:20-16:50 November 7th
VENUE	JuXian Function Room @Level 2（2楼聚贤厅）
SPEAKER	Shujuan Liu, Yangtze Laboratory

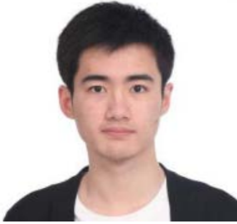
ABSTRACT

Artificial intelligence, data center, automatic driving and other applications put forward higher requirements for chip performance. However, the "Moore's Law" is currently approaching the physical limit. The development of IC technology has encountered physical and cost challenges. Chiplet can achieve heterogeneous integration of chips with different processes and functions through advanced 2.5D/3D interconnect technology, forming a high-performance chip system that can be flexibly configured to meet the high-performance requirements. This report will introduce the opportunities and challenges faced by the advanced 2.5D/3D interconnect technologies, pointing out that these technologies for the system integration of CPU/GPU, memory, sensor and other functional chips can break through the limitations of traditional packaging interconnect methods on data transmission rate and energy efficiency. The hybrid bonding of W2W/D2W can lead to innovative integrated system, providing higher density, faster speed, greater bandwidth, and lower power consumption solutions.

BIOGRAPHY

Liu Shujuan is the leader of Science Research Institute in Yangtze Laboratory. She received her Ph.D. degree from Xi'an Jiaotong University. She mainly engages in research on advanced packaging Cutting-edge technology, she is now responsible for the advanced packaging technology simulation platform, catering to the computational and simulation needs at the materials/device/chip/wafer level, using data and algorithms to drive the process optimization and technology iteration.

TITLE	**Research on the Reliability of 2.5D/3D IC under Multi Physical Field Coupling**
TIME	16:50-17:20 November 7th
VENUE	JuXian Function Room @Level 2（2楼聚贤厅）
SPEAKER	Jiahao Zhou, DeTooLIC Technology



ABSTRACT
Against the backdrop of computing power demands such as artificial intelligence and autonomous driving, advanced packaging plays an increasingly important role in improving chip integration, shortening chip distance, and optimizing performance. However, the smaller thermal space and higher power density within a 2.5D/3D chip will generate more complex physical fields such as electricity, heat, and stress. Therefore, this article discusses the reliability analysis of 2.5D/3D integrated circuits from the perspectives of reasons and methods. In addition, the prospects of advanced packaging multi field simulation were discussed, providing reference for the reliability research of advanced packaging.

BIOGRAPHY
Zhou Jiahao graduated from Zhejiang University with a major in Information Engineering, during which he studied Si-Pi Simulation Analysis at the EMC Lab of Missouri University of Science and Technology in the United States. After graduation, he continued to join the laboratory team to research electromagnetic field direction algorithms and led the development of SonicPower, a power chip power integrity simulation tool. Exploring innovative simulation solutions for chips and advanced packaging scenarios in response to domestic EDA bottlenecks, and assisting in the construction of EDA ecosystem.

OVERVIEW OF SESSIONS VII

SESSIONS	AI assisted EMC/SI/PI Technologies
VENUE	Room 1: JiangNan Function Room @Level 2（2 楼江南厅）
TIME	08:30-11:30 November 8th
SESSION CHAIR	Xiuqin Chu, Xidian University Hanzhi Ma, Zhejiang University
INVITED TALK	**A Comprehensive Design Methodology for Chiplet-based 2.5-D Integrated Circuits** *Wensheng Zhao, Hangzhou Dianzi University* **Computer Vision Assisted Metamaterial Systems for Self-adaptive Wireless Communications** *Wenxuan Tang, Southeast University* **Space Mapping Techniques for EM Design Optimization** *Feng Feng, Tianjin University* **Machine Learning-Enabled Fast Electromagnetic Modeling and Optimization Approaches to Metasurface Design** *Jianan Zhang, Southeast University* **High-Speed Circuit Transient Simulation based on Machine Learning Techniques** *Hanzhi Ma, Zhejiang University* **Application of Machine Learning in Signal Integrity** *Xiuqin Chu, Xidian University*

TITLE	**A Comprehensive Design Methodology for Chiplet-based 2.5-D Integrated Circuits**
TIME	08:30-09:00 November 8th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Wensheng Zhao, Hangzhou Dianzi University

ABSTRACT

Thermal issues and power integrity problems have long been recognized as critical challenges in the design of 2.5-D integrated microsystems. In this paper, a thermal and power integrity co-optimization framework, consisting of a sequential two-stage design and driven by the improved adaptive genetic algorithm, is proposed. In the first stage, the thermally-aware placement, comprehending key design indexes encompassing area, peak temperature, temperature uniformity, and wire routing constrained by multicommodity flow constraints of multi-dies, is addressed. In the second stage, the transmission matrix method is first utilized to characterize the impedance of the hierarchic power delivery network based on the determined chip architecture from the first stage. Then, the initial impedance of the observed port, directly correlated with simultaneous switching noise, is reduced by the layout optimization of on-chip decoupling capacitances. Following this, a benchmark case is established to validate the design framework and its embedded algorithm from multiple perspectives. The results demonstrate that the proposed framework is capable of generating superior solutions compared to mainstream algorithms. Additionally, the proposed design methodology is compared with that of the state-of-the-art studies, revealing that this work bridges the thermal and power integrity domains. This accomplishment provides a novel design paradigm of electronic design automation tools targeting large-scale and highly complex 2.5-D integrated microsystems in the future.

BIOGRAPHY

Wen-Sheng Zhao (Senior Member, IEEE) received the B.E. degree from Harbin Institute of Technology, Harbin, China, in 2008, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 2013.

During his Ph.D. study, he was with the National University of Singapore, Singapore, from 2010 to 2013, where he was involved in the development of TSV-based 3D ICs. He was a visiting scholar with the Georgia

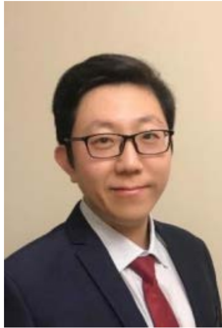
Institute of Technology, Atlanta, USA, from 2017 to 2018. He is currently a full professor with Hangzhou Dianzi University, Hangzhou, China. He has published 3 books, 5 book chapters, and 150 SCI journal articles (including 88 IEEE papers). He holds more than 50 authorized patents. His current research interests include IC interconnect and packaging, passive components, and electronic design automation.
He is a Senior Member of Chinese Institute of Electronics. He serves as associate editor/editorial member/guest editor for several journals including IEEE ACCESS, Microelectronics Journal, Chinese Journal of Electronics, Journal of Microwaves, Electronics, and Micromachines.

TITLE	**Computer Vision Assisted Metamaterial Systems for Self-adaptive Wireless Communications**
TIME	09:00-09:30 November 8th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Wenxuan Tang, Southeast University

ABSTRACT
Future wireless communication puts forward new requirements for the intelligent services based on user positioning and identification. In this work, we propose that intelligent communication systems and smart antennas based on reconfigurable metamaterials with assistance of computer vision can operate efficiently in closed loop without human intervention. This kind of system is composed of digital programmable metasurfaces or reconfigurable spoof surface plasmons, combined with the depth camera to acquire target images at high speed and in real time. Computer vision is adopted to detect the position of moving targets and identify their classification. This report introduces three kinds of computer vision-assisted metamaterial systems. First, intelligent tracking and communication systems based on coding metasurface and computer vision is composed and realized. Secondly, based on the spoof surface plasmon polaritons (SSPPs), an external perceptive smart leaky wave antenna is realized with self-adaptive working state and self-adjusting beam tracking. Thirdly, a multi-user balloon communication system based on flexible metamaterials is demonstrated.

BIOGRAPHY
Dr. Wenxuan Tang received the B.Sc. and M.Sc. degrees from Southeast University, Nanjing, China, in 2006 and 2009, respectively, and the Ph.D. degree in electromagnetics from the Queen Mary University of London, London, U.K., in 2012. In 2012, she joined the School of Information Science and Engineering, Southeast University, where she is currently a professor with the State Key Laboratory of Millimeter Waves. Her current research interest focuses on the metamaterials and their applications, and microwave devices and systems. She is a senior member of the Chinese Institute of Electronics (CIE), and a committee member of the CIE Radio Propagation Society. She is also the associate editor of Antennas and Wireless Propagation Letters and EPJ Applied Metamaterials. She has co-authored more than 80 papers and edited one book. She has been the principal investigator of several research projects, including tasks of the National Key Research and Development Program of China and projects of the National Natural Science Foundation of China.

TITLE	**Space Mapping Techniques for EM Design Optimization**
TIME	09:30-10:00 November 8th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Feng Feng, Tianjin University



ABSTRACT
Space mapping (SM) is a recognized electromagnetic (EM) optimization methodology in the microwave area. The space mapping concept combines the computational efficiency of coarse models with the accuracy of fine models. The coarse models are typically empirical functions or equivalent circuit models, which are computationally efficient. However, such models are often valid only in a limited region of input space, beyond which the model predictions become inaccurate. On the other hand, detailed or "fine" models can be provided by an electromagnetic (EM) simulator, or even by direct measurements. The detailed models are accurate, but can be expensive (e.g., CPU-intensive simulations). The space mapping technique establishes a mathematical link between the coarse and the fine models and directs the bulk of the CPU-intensive computations to the coarse model, while preserving the accuracy offered by the fine model. In this talk, the concept and recent advances in space mapping techniques for EM design optimization will be introduced and discussed.

BIOGRAPHY
Feng Feng is a Professor with the School of Microelectronics at Tianjin University, Tianjin, China. His research focuses on electromagnetic (EM)/multiphysics parametric modeling and design optimization algorithms, and has authored/co-authored over 150 journal and conference papers, including over 40 papers published in IEEE Transactions on Microwave Theory and Techniques.
Dr. Feng serves as the vice chair of the Technical Committee on Design Automation (TC-2) of the IEEE Microwave Theory and Technology Society (IEEE MTT-S). He serves as a guest editor of IEEE Microwave Magazine and a reviewer for many IEEE scientific publications, including IEEE Transactions on Microwave Theory and Techniques, IEEE Microwave and Wireless Technology Letters, etc. He served as the General Chair, 2021 IEEE MTT-S Young Professionals Workshop on Electromagnetic Modeling and Optimization (EMO 2021).

TITLE	**Machine Learning-Enabled Fast Electromagnetic Modeling and Optimization Approaches to Metasurface Design**
TIME	10:00-10:30 November 8th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Jianan Zhang, Southeast University

ABSTRACT
Today's metasurface elements typically have complex electromagnetic (EM) structures, making numerical optimization of metasurface elements a critical and highly challenging task. Traditional commercial EM simulation software optimizers need to repeatedly modify the topology or geometric parameter values of units and perform a large number of full wave EM simulations, which is time-consuming and memory-intensive.
This talk will first briefly introduce how traditional pure data-driven machine learning methods are applied to metasurface design, and then discuss more advanced physics-driven machine learning algorithms, namely the neuro-CMT method, recently proposed by our research group and its application progress in the rapid design of passive metasurface absorbers. Next, the talk will cover a novel surrogate-model-assisted optimization method incorporating deep learning techniques and the microwave network theory to enable rapid and automated design of reconfigurable intelligent metasurfaces.

BIOGRAPHY
Jia Nan Zhang received the B.Eng. degree in Tianjin University, Tianjin, China, in 2013. He received the Ph.D. degree in the School of Microelectronics at Tianjin University, Tianjin, China, and the Department of Electronics at Carleton University, Ottawa, ON, Canada, in 2020.
From 2020 to 2022, he was a Post-Doctoral Research Associate in the Department of Electronics at Carleton University, Ottawa, ON, Canada. In January 2022, he joined the State Key Laboratory of Millimeter Waves at

Southeast University, Nanjing, China, where he is currently a Professor. He has authored/co-authored over 80 publications in prestigious microwave journals/conferences. He contributed to the Encyclopedia of Surrogate Modeling for High-Frequency Design: Recent advances (World Scientific, 2021), and Uncertainty Quantification of Electromagnetic Devices, Circuits, and Systems (IET, 2021). His research interests include machine-learning approaches to microwave design, surrogate modeling and surrogate-assisted optimization, finite element analysis in EM, and quantum computing with applications to EM problems.
Dr. Zhang is a member of IEEE, IEEE Microwave Theory and Techniques Society (IEEE MTT-S), and IEEE Antennas and Propagation Society (IEEE AP-S). He served as the general chair of 2022 IEEE MTT-S Young Professionals Workshop on Electromagnetic Modeling and Optimization (EMO 2022). He is a reviewer of a number of renowned microwave journals, including IEEE TMTT, IEEE TCAS-I, IEEE AWPL, and IEEE MWTL.

TITLE	**High-Speed Circuit Transient Simulation based on Machine Learning Techniques**
TIME	10:40-11:10 November 8th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Hanzhi Ma, Zhejiang University

ABSTRACT

The relentless advancements in integrated circuit fabrication technologies and the growing complexity of modern electronic devices have led to continuous improvements in data transmission rates, making signal integrity (SI) a critical concern in electronic system design. Transient simulation is crucial for accurate signal integrity modeling in high-speed links. This approach captures the dynamic temporal behavior of circuit components and encompasses nonlinear signal distortions. However, conventional transient simulation techniques and associated simulation tools still face challenges when dealing with the substantial computational demands posed by highspeed links characterized by extremely long input bit patterns.
Artificial intelligence (AI) methods provide innovative solutions to the significant computational challenges in transient modeling of high-speed links. However, current AI-based approaches face two major issues: the time-consuming nature of model training and the isolated operation of existing neural network methods. This presentation will address these challenges and propose potential solutions for transient simulation of high-speed links.

BIOGRAPHY

Hanzhi Ma is currently an assistant professor at Zhejiang University and an adjunct assistant professor at University of Illinois Urbana-Champaign. She received the B.S. degree and Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2017 and 2022. Her research interests involve electromagnetic compatibility, signal integrity, and power integrity, with a focus on electronic automation design methods for electromagnetic integrity in high-performance integrated circuits. She has twice received the President's Memorial Award from IEEE Electromagnetic Compatibility Society and has been selected as the Young Professional Ambassador of IEEE Electromagnetic Compatibility Society. She won the Excellent Doctoral Thesis Award from Chinese Institute of Electronics and the Best Student Paper Award at the Asia-Pacific International Symposium on Electromagnetic Compatibility. She has served as a Guest Editor for IEEE Transactions on Components, Packaging and Manufacturing Technology and as a TPC member and session chair for more than 10 international conferences (including IEEE EDAPS 2020-2024, IEEE EMC Symposium 2024, APEMC 2022-2024, and ACES 2023-2024).

TITLE	**Application of Machine Learning in Signal Integrity**
TIME	11:10-11:40 November 8th
VENUE	JiangNan Function Room @Level 2（2 楼江南厅）
SPEAKER	Xiuqin Chu, Xidian University

ABSTRACT

With the rapid development of new data centers, the global computing power market continues to be hot, and the computing servers and network switches with large bandwidth and low latency support the underlying hardware operation. How to find the best system SI solution in the highly complex channel design and multiple active balanced configurations to achieve high-speed signal transmission with low bit error rate is one of the core challenges of hardware design. Aiming at these problems, this topic will introduce the future challenges and research hotspots of high-speed signal integrity, the latest application of machine learning in signal integrity and our research achievements, including nonlinear system response prediction, channel equalization coefficient and response prediction, passive channel multi-variable parameter combination optimization, etc. And discuss with you the future application direction and opportunities of machine learning in the field of signal integrity, and jointly explore more technical highlights to provide greater help to the cost and performance of future products.

BIOGRAPHY

Chu Xiuqin, is a professor and doctoral supervisor of Xidian University, Deputy Director of Key Laboratory of Ultra-High-Speed Circuit Design and Electromagnetic Compatibility of Ministry of Education, Executive Deputy Director of Circuit CAD Institute, leader of Signal Integrity Analysis team of Xidian University.

Over the years, she has focused on the research of high-speed circuit signal integrity and power supply integrity, and has published nearly 10 translated books and monographs in SI/PI field together with his team. In 2016-2017, she visited EMC Laboratory of Missouri University of Science and Technology in the United States, won the best paper award of IEEE EMC of IC International Conference in 2019, published more than 50 academic papers in domestic and foreign journals and international conferences, and won the second prize of Science and Technology Progress of Shaanxi Province as the first completed person. She has presided over dozens of national key research and development programs, National Natural Science Foundation projects, space funds and scientific research achievements transformation projects.

OVERVIEW OF SESSIONS VIII

SESSIONS	Electromagnetic Modeling, Design, and Measurement of Circuits, Devices, and Metamaterials
VENUE	Room 2: YuanShi Function Room @Level 2（2楼院士厅）
TIME	08:30-12:00 November 8th
SESSION CHAIR	Xiong Chen, Xi'an Jiaotong University Ling Zhang, Zhejiang University
INVITED TALK	**Progess in the Development of Silicon-Based Terahertz Radiation Sources and Phased Array Chips** *Liang Gao, Southeast University* **Seeking Shapes of Planar Interconnects with Higher Flexibility** *Xiaojie Ma, Beijing Huairou Laboratory* **Preliminary Conceptual Study of Novel Materials, Devices and Test Equipments for Electromagnetic Compatibility** *Yusheng Hu, Jimei University* **Analysis of Power Device Switching Characteristics and EMI Optimization of Motor Drivers** *Yongning He, Xi'an Jiaotong University* **Evaluation Method for Roughness Performance of Copper Foil** *Yade Fang, DeTooLIC Technology* **Capacitance Impact on Passive Intermodulation Generation with its Measurement** *Xiong Chen, Xi'an Jiaotong University*

TITLE	**Progess in the Development of Silicon-Based Terahertz Radiation Sources and Phased Array Chips**
TIME	08:30-09:00 November 8th
VENUE	YuanShi Function Room @Level 2（2楼院士厅）
SPEAKER	Liang Gao, Southeast University

ABSTRACT

The terahertz (THz) spectrum (0.1 THz – 10 THz) plays a crucial role in high-speed communications for future 6G, as well as in non-invasive imaging and spectroscopy. Among various technologies, silicon-based integrated circuit technology stands out for its commercial viability and high yield, making it attractive for compact and cost-effective terahertz applications. Terahertz signal sources are vital components of most terahertz systems. However, generating high-power terahertz signals above 300 GHz poses significant challenges, as the maximum oscillation frequency (fmax) of transistors based on CMOS technology is around 300 GHz. In this talk, I will present our designed coherent terahertz radiator array chips in CMOS process. By employing various innovative array architectures and design methods, we have progressively pushed the boundaries of output frequency and power in CMOS technology, successfully achieving milliwatt-level radiation power around 700 GHz. This milestone sets a new record for the highest output power in silicon-based technology above 300 GHz. Furthermore, large-scale terahertz phased array systems can effectively mitigate the high path loss associated with the terahertz frequency range, facilitating longer-distance terahertz communication and sensing applications. After addressing the technical challenges of generating high-power terahertz signals using silicon-based technology, I will also share our research progress on silicon-based terahertz phased array chips.

BIOGRAPHY

Liang Gao received the B.Eng. degree in electronic information science and technology from Sun Yat-sen University, Guangzhou, China, in June 2018 and the Ph.D. degree in electrical engineering from City University of Hong Kong, Hong Kong, in July 2022. From August 2022 to February 2023, he was with the State Key Laboratory of Terahertz and Millimeter Waves, City University of Hong Kong as a postdoctoral

fellow. In March 2023, he joined the CoSMIC Lab. at Columbia University as a postdoctoral research scientist. He is currently a Professor with the School of Information Science and Engineering, Southeast University, Nanjing, China. His current research interests include integrated circuits and systems, and on-chip antenna design at millimeter-wave and terahertz frequencies. He has co-authored more than 10 journal and conference papers, including 3 JSSC and 1 ISSCC.

TITLE	**Seeking Shapes of Planar Interconnects with Higher Flexibility**
TIME	09:00-09:30 November 8th
VENUE	YuanShi Function Room @Level 2（2楼院士厅）
SPEAKER	Xiaojie Ma, Beijing Huairou Laboratory

ABSTRACT

The damage and fracture of interconnects often arise from thermal loadings during the production and service process. Increasing the flexibility of interconnects can mitigate these problems. The rational design with higher property usually calls for the calculus of variations. However, the hard nonlinearity involved in the geometry and flexibility invalidates the typical methods, such as applying Euler-Lagrange differential equation and Rayleigh-Ritz method, even when the interconnects are planar. Having observed abundant samples, we will excitingly show that the superior shapes of planar interconnects with different lengths can all be approximately transformed into a unified profile. An analytical proof will be subsequently presented, illustrating that the normalized global optimum solutions are indeed close to the unified profile. Moreover, even if there exists a limitation on the minimum curvature radius in engineering scenes, the unified profile is still useful. Finally, we will imply that our paradigm should extend to other optimization problems involving calculus of variations with hard nonlinearity.

BIOGRAPHY

Xiaojie Ma is an R&D staff at Beijing Huairou Laboratory. He earned a bachelor degree from Hebei University of Technology in 2018, majoring in Civil Engineering. Upon earning a Ph.D. degree in Solid Mechanics from Peking University, in 2023, Ma joined Beijing Huairou Laboratory. His research centers on the mechanical behavior of materials and structures. Basic processes include fracture and deformation, arising from various physical fields (e.g., mechanical, thermal, and electrical stress). In retrospect, his paradigm is clear: finding the mechanism behind the complex phenomena and then using it to actively control the behavior for potential application. His publications cover mechanics, physics, and materials science.

TITLE	**Preliminary Conceptual Study of Novel Materials, Devices and Test Equipments for Electromagnetic Compatibility**
TIME	09:30-10:00 November 8th
VENUE	YuanShi Function Room @Level 2（2楼院士厅）
SPEAKER	Yusheng Hu, Jimei University

ABSTRACT

With the rapid development of electronic systems to the direction of miniaturization, lightweight, high-frequency and high integration, there is an urgent need for wide frequency band, thin-film and high-performance advanced EMC materials, new electronic components as well as new EMC test equipment.This talk introduces the conceptual design of new materials for shielding and filtering based on metamaterials, microstructures and complex interconnect technologies. Taking co-inductance EBG, metal/dielectric composite EBG, and cond-capacitor as examples, we illustrate their excellent performance and their applications in EMI/SI/PI.Finally, a new mini-TEM cell for IC EMC measurement with upper limit frequency up to 6 GHz or more is introduced.

BIOGRAPHY

Yusheng Hu received the Ph. D. from Southeast University, Nanjing, China in 2004. From Sep. 2004 to Aug. 2007, he was with Nanjing University of Aeronautics and Astronautics, as a postdoctoral research fellow. From

Sep. 2010 to Mar. 2011, he was a visiting scholar in EMC Laboratory of Missouri University of Science and Technology. From Oct. 2014 to Sep. 2015, he is in Department of Electronics and Telecommunications, Politecnico Di Torino, Torino, Italy, as a visiting scholar. He is currently a professor with Jimei University, Xiamen, China. His research areas of interest include numerical modeling of EMC/SI/PI for complex high-speed digital systems, computational electromagnetics, and metamaterials, etc.

TITLE	**Analysis of Power Device Switching Characteristics and EMI Optimization of Motor Drivers**
TIME	10:00-10:30 November 8th
VENUE	YuanShi Function Room @Level 2（2 楼院士厅）
SPEAKER	Yongning He, Xi'an Jiaotong University

ABSTRACT

This report explores the analysis of the switching characteristics of power devices and their optimization for electromagnetic interference (EMI) in motor drivers. With the rapid development of motor drive technology, the application of power devices in motor control has become increasingly widespread. However, high-frequency noise and electromagnetic interference generated during switching processes significantly impact system performance and stability. This study analyzes the switching characteristics of power devices and identifies the key factors affecting EMI. Based on these analytical results, optimization strategies are proposed to effectively reduce EMI and enhance overall system performance. Additionally, practical case studies are presented, demonstrating that these optimization measures significantly improve the electromagnetic compatibility of motor drivers.

BIOGRAPHY

Yongning He received the M. S. degree in 2000 and Ph. D degree in 2005 from Xi’an Jiaotong University, Xi’an, China. She is a professor and doctoral supervisor at the School of Electronics and Information, Xi'an Jiaotong University. His main research areas include semiconductor sensor devices and their integrated systems, wide-bandgap semiconductor devices and their reliability issues, microwave devices and their reliability issues, and cold plasma sources and their application devices.

TITLE	**Evaluation Method for Roughness Performance of Copper Foil**
TIME	10:40-11:10 November 8th
VENUE	YuanShi Function Room @Level 2（2 楼院士厅）
SPEAKER	Yade Fang, DeTooLIC Technology

ABSTRACT

With the development of semiconductor technology, signal rates are also increasing. The influence of surface roughness on signal loss is also receiving increasing attention. The demand for analyzing the roughness of signal copper foil from the perspective of actual PCB is also increasing. SRTool is a tool that can analyze the surface roughness of copper foil based on actual slicing.

BIOGRAPHY

Yade Fang is an expert in signal integrity and power integrity simulation, especially skilled at high-speed simulation for DDR, PCIE, etc. He is a senior application engineer at DetooLIC and serves almost 20 customers in East China. Prior to working in DetooLIC, he worked at CXMT.

TITLE	**Capacitance Impact on Passive Intermodulation Generation with its Measurement**
TIME	11:10-11:40 November 8th
VENUE	YuanShi Function Room @Level 2（2楼院士厅）
SPEAKER	Xiong Chen, Xi'an Jiaotong University

ABSTRACT

This report summarizes the nonlinear distortion mechanism on coaxial system including coaxial adapters, connectors and cables, some modeling methods for the nonlinear products are demonstrated, then a set of mitigation methods to suppress passive nonlinear distortion are demonstrated, including the fabrication improvements and active signal cancelling methods.

BIOGRAPHY

Xiong Chen received his Ph.D. degree in electrical engineering from Xi'an Jiaotong University, he is currently an outstanding researcher (tenured associated professor) in Xi'an Jiaotong University. Dr. Chen has authored over 60 journals or conference publications and patents (includes US patent) on MW/RF component design and reliability, also serve as the Chair for several international MW/RF conferences and workshops since 2019. His current research interests include MW/RF circuit design, high power MW/RF device, MW/RF nonlinear distortion effect in wireless communication.

OVERVIEW OF SESSIONS IX

SESSIONS	ESD/EMI Techniques for Electronic Systems
VENUE	Room 3: JuXian Function Room @Level 2（2楼聚贤厅）
TIME	08:30-11:00 November 8th
SESSION CHAIR	Shurong Dong, Zhejiang University Fayu Wan, Nanjing University of Information Science and Technology
INVITED TALK	**Charged Device Model ESD Sensitivity Tester Design and Application** *Fayu Wan, Nanjing University of Information Science & Technology* **Review and Case Study of ESD Simulation** *Qiang Cui, Zhejiang University's College of Integrated Circuits* **Modeling the Transmission Characteristics of ESD signal in a Non-linear System** *Guang-Xiao Luo, North China Electric Power University* **EMI Issues and Challenges in Consumer Electronics** *Kaixiang Zhu, Honor Device Co., Ltd* **Study on Radiation Interference from High-speed Railway Pantograph-catenary Detachment arc Considering the Train Speed Influence** *Ke Huang, Southwest Jiaotong University*

TITLE	**Charged Device Model ESD Sensitivity Tester Design and Application**
TIME	08:30-09:00 November 8th
VENUE	JuXian Function Room @Level 2（2楼聚贤厅）
SPEAKER	Fayu Wan, Nanjing University of Information Science & Technology

ABSTRACT

We present an electrostatic device (ESD) tester with particularly high sensitivity for the charged device model (CDM) by incorporating empirical equivalent circuit (EC) parameters. The tester is implemented by using software and hardware system. The tester feasibility study involves circuit theoretical analysis and simulation enabling to investigate the influence of EC parameters on the discharge signal waveform. High-precision and automated ESD sensitivity are utilized to develop the proposed testing system. As proof of concept, various common electronic components are tested. The performed experiment reveals that the CDM discharge signal is influenced not only by the DUT's capacitance, but also by the packaging structure and pins for different functions. The explored measurement results highlight the importance of considering different pins for electronic device ESD protection. The present study is industrially useful to enhance the ESD immunity during the design of electronic devices or chips by considering their circuit connections.

BIOGRAPHY

Wan Fayu, a professor and doctoral supervisor, received his Ph.D. from the University of Rouen in France in 2011. From 2011 to 2013, he conducted postdoctoral research at the Electromagnetic Compatibility Laboratory of the University of Missouri-Rolla. His research directions encompass environmental effects of electrostatic discharge, electromagnetic hazard effects, and negative group delay circuits. He has undertaken five national-level scientific research projects including one National Key Research and Development Program of China. Moreover, he has published over 100 SCI journals such as IEEE TIE, TIM, TEMC, TCAS, and TCAD, and has been awarded 25 invention patents. He has also participated in formulating five national standards in the fields of electromagnetic compatibility and electrostatic discharge.

TITLE	**Review and Case Study of ESD Simulation**
TIME	09:00-09:30 November 8th
VENUE	JuXian Function Room @Level 2（2楼聚贤厅）
SPEAKER	Qiang Cui, Zhejiang University's College of Integrated Circuits

ABSTRACT

Electrostatic discharge (ESD) is a major threat to integrated circuits (ICs)' reliability, and the technology computer-aided design (TCAD) simulation is the key method to analyze ICs' on-chip ESD protection ability. To be ready for production, the ICs must pass various ESD test standards, including MIL-STD-883, IEC 6100-4-2, and AEC-Q100, as well as transmission line pulsing with different rise times and pulse widths. The TCAD simulation work reported in the existing literature typically only focuses on a narrow scope, such as steady state current-voltage (IV) characteristics, transient analysis, electron-hole contour, or temperature contour.
The fragmented research on TCAD simulation failed to analyze on-chip ESD protection systematically. This presentation developed a thorough TCAD simulation method covering all major ESD standards and models to fill this research gap. It elaborated the method with a silicon controlled rectifier (SCR) based protection device design. The abovementioned simulation method includes steady-state analysis, transient analysis, temperature effect, and circuit-device mixed-mode setup. This TCAD simulation method can effectively help designers analyze and design protection devices for ICs against ESD related reliability issues.

BIOGRAPHY

Dr. Qiang Cui is the Tenure-Track Professor of Zhejiang University's College of Integrated Circuits. Dr. Cui has over 15 years of experience in the semiconductor industry (Apple, Qorvo) and research institutes (Massachusetts Institute of Technology, University of Central Florida). He has led or designed several strategic integrated circuits widely used in wireless products. Dr. Cui is a senior member of lEEE and serves on the reviewer panel of several lEEE journals such as IEEE Transaction on Electron Devices, IEEE Electron Device Letters, IEEE Transaction on Device and Materials Reliability, Solid State Electronics and Microelectronics Reliability, and so on. Dr Cui’s current research interests include automotive ESD protection, wireless communication ICs, high speed I/O circuits and mixed signal IC design.

TITLE	**Modeling the Transmission Characteristics of ESD signal in a Non-linear System**
TIME	09:30-10:00 November 8th
VENUE	JuXian Function Room @Level 2（2楼聚贤厅）
SPEAKER	Guang-Xiao Luo, North China Electric Power University

ABSTRACT

A frequency-domain method is proposed to model the transmission characteristics of a system including internal transient voltage suppressor (TVS) device under ESD pulse. The frequency-domain model of the non-linear system is obtained by using the Fourier transform of the injecting TLP signal and the receiving response waveform at the IC port. This method is validated by the other level of TLP signal and the IEC-61000-4-2 excitation signal.

BIOGRAPHY

Guang-Xiao Luo (Senior Member, IEEE) received B.Sc. degree in communication engineering, M.Sc. degree in system of communication and information, and Ph.D. degree in electrical engineering from North China Electric Power University, China, in 2000, 2003 and 2015, respectively.
From September 2018 to July 2020, he was a Postdoctoral Researcher (supported by China Scholarship Council) with the Electromagnetic Compatibility Laboratory, Missouri University of S&T, Rolla, MO, USA. In 2003, he joined the School of Electrical and Electronic Engineering, North China Electric Power University. His research interests include circuit modeling, numerical simulations and measurements of EMC and ESD.

TITLE	**EMI Issues and Challenges in Consumer Electronics**
TIME	10:00-10:30 November 8th
VENUE	JuXian Function Room @Level 2（2楼聚贤厅）
SPEAKER	Kaixiang Zhu, Honor Device Co., Ltd

ABSTRACT

With the continuous improvement of the integration and functionality of consumer electronics products, and the simultaneous continuous growth of network format requirements and high data transmission rates, the inner system electromagnetic compatibility problems of the products, such as RFI and the interference of radio frequency to multimedia modules, have become increasingly prominent and have become important influencing factors affecting product development cycles, architectural designs, and functional designs. Meanwhile, the characteristic of mass production makes batch consistency and cost factors that must be considered in addressing the electromagnetic compatibility problems of consumer electronics products. This report mainly introduces the main EMI problems in current consumer electronics products such as mobile phones, as well as the challenges that can be expected in the foreseeable future.

BIOGRAPHY

Kaixiang Zhu received the B.S. degree and the Ph.D. degree from Beihang University, Beijing China, in 2013 and 2019. He is currently a Senior Engineer with Honor Device, working towards RF interference, susceptibility of multimedia module and other EMI problems in terminal products.

TITLE	**Study on Radiation Interference from High-speed Railway Pantograph-catenary Detachment arc Considering the Train Speed Influence**
TIME	10:40-11:10 November 8th
VENUE	JuXian Function Room @Level 2（2楼聚贤厅）
SPEAKER	Ke Huang, Southwest Jiaotong University

ABSTRACT

High-speed railway is a crucial part of modern transportation, offering speed, comfort, punctuality and safety. However, the overhead contact system used to receive electric power can cause detachment arcs on train roofs, creating electromagnetic interference (EMI) that impacts railway electromagnetic compatibility (EMC). This study explores how train speed affects arc radiation characteristics through modeling, calculations, and field tests, addressing gaps in previous research and the need for faster train. At first, a distributed parameter model of vehicle-grid power supply system is developed using ATP-EMTP software. This model incorporates two common detachment arc scenarios: traversing ordinary hard points and split-phase insulators. It calculates transient arc voltages and currents to determine arc radiation intensity in each case. Subsequently, field tests are conducted to measure the electric field strength from arcs at various speeds over ordinary hard points and split-phase insulator. An improved least squares model fits the test data to create arc amplitude-frequency curves. By comparing the test data with theoretical calculations, the influence of train speed is evaluated. Furthermore, EMI limits for various frequency bands are calculated, with a particular focus on airport. Proposed speed limits for trains passing through areas sensitive to EMI are included.

BIOGRAPHY

Ke Huang (Member, IEEE) was a visiting scholar in EMC Laboratory, Missouri University of Science and Technology, Rolla, MO, USA, from 2018 to 2019. He received the Ph.D. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2020. From 2021 to April 2024, he was a Post-Doctoral Fellow at the National Maglev Transportation Engineering R&D Center, Tongji University, Shanghai, China. Dr. Huang is currently an associate researcher working at EMC Laboratory and National Rail Transit Electrification and Automation Engineering Technique Research Center, Southwest Jiaotong University. He has 10 articles published in the SCI journals as the first author, including IEEE Transactions on Transportation Electrification and IEEE Transactions on Instrumentation & Measurement, which are top journals in the field of electrified transportation. He has secured approval for 3 research projects in the last 3 years, and two of them are related to the EMC issues of rail transit. His main research interests involve Electromagnetic compatibility protection for transportation and Optimization of traction power supply system for high-speed railway and urban rail transit.

PANEL DISCUSSION I

TOPIC	Technical Trend and Future Direction in the EDA of High Speed and High Bandwidth Interconnect
TIME	11:00 – 12:00, November 7th
VENUE	Room 2: YuanShi Function Room @Level 2（2 楼院士厅）
PANEL CHAIR	Zhufei Chu, Professor, Ningbo University
INVITED PANELIST	Haisan Wang, AE Director, Cadence Jie Liu, EDA Product Planning Representative, Qiyunfang Technology Co., LTD. Davy Dai, Product Marketing Director, UniVista Yanwu Wang, Senior Director, DeTooLIC Technology Ting-Jung Lin, Associate Professor, Engineering Research Center of Chiplet Design and Manufacturing of Zhejiang Province Peng Zhao, Chief Scientist, Faraday Dynamics Co., Ltd.

KEY TOPICS INCLUDE:

- **Global Market Demands**: EDA of high-speed and high bandwidth interconnects for Chiplet, data centers, AI systems, and supercomputing infrastructure.
- **Innovative Solutions and Future Trends**: Exploring cutting-edge solutions and technological advancements to meet the industry's demands.

BIOS OF PANEL CHAIR

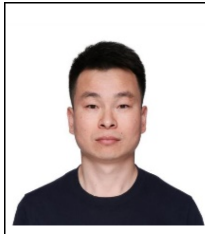
Zhufei Chu, Professor, Ningbo University

Zhufei Chu received the B.S. degree in electronic engineering from Shandong University, Weihai, China, in 2008 and the M.S. and Ph.D. degrees in communication and information system from Ningbo University, Ningbo, China, in 2011 and 2014, respectively. He was a Postdoctoral Fellow at the \'Ecole Polytechnique F\'ed\'ederale de Lausanne (EPFL) during 2016 to 2017. He is currently a Professor with Ningbo University, Ningbo, China.

He serves as the proceedings chair (2019-2021) and finance chair (2022-2023) of the international workshop on logic and synthesis (IWLS), and also technical program committee members for design automation conference (DAC), IWLS, and international conference on VLSI design (VLSID).

He is actively maintaining the logic synthesis framework ALSO (https://github.com/nbulsi/also).His current research interests include the many aspects of logic synthesis and its applications.

BIOS OF INVITED PANELIST



Haisan Wang, AE Director, Cadence

Haisan Wang is an AE director from Cadence Multi-Physics System Analysis (MSA) service AE team. He mainly focuses on performing high performance chip system design by co-design and co-simulation technology. Prior to joining Cadence, he worked at Sigrity and Huawei.

Jie Liu, EDA Product Planning Representative, Qiyunfang Technology Co., LTD.

Jie Liu, master's degree, graduated from the School of Huazhong University of Science and Technology.He is currently the EDA product planning representative of Qiyunfang Technology Co., LTD. He has been working in the field of EDA applications for more than 18 years. He has a deep understanding of board interconnection design, familiar with HF PCB laminating, production process, DFM and other related design elements of industry present situation and development, comprehensive PCB signal and EMC requirements for board level planning and analysis.

He is proficient in PCB related SI / PI / EMC analysis, with rich experience of RF microwave PCB, RF passive devices, optical module design experience, proficient in radio frequency and high-speed signal board level, packaging level design analysis and planning. He has obtained 4 technology patents.

Davy Dai, Product Marketing Director, UniVista

Responsible for planning and marketing system-level EDA products, Davy boasts 20 years of experience in PCB board-level and package-level design and support, as well as extensive experience in the use and development of EDA products. Collaborating with UniVista powerful R&D team, Davy focuses on the system-level electronic design market, aligning with industry best practices to provide exceptional commercial-grade solutions.

Yanwu Wang, Senior Director, DeTooLIC Technology

Yanwu Wang, Senior director of High-speed and customer technical support department in DeTooLIC Technology, He is focusing on signal and power integrity design, optimization and system solution, had 15+ years of experience in the field of high speed SerDes design and DDR design on computer and server products. Before join DeTooLIC Technology, he was responsible for high speed system design and product development in multiple companies.

Ting-Jung Lin, Associate Professor, Engineering Research Center of Chiplet Design and Manufacturing of Zhejiang Province

Dr Lin is currently an associate professor at Ningbo Institute of Digital Twin, Eastern Institute of Technology. She is also a core member of the Engineering Research Center of Chiplet Design and Manufacturing of Zhejiang Province and an R&D director of BTD Technology Co., Ltd. She got her PhD from Princeton University in 2014 and worked with Synopsys' verification group from 2014 to 2017. Her research interests include AI-driven circuit design automation and characterization.

Peng Zhao, Chief Scientist, Faraday Dynamics Co., Ltd.

Peng Zhao, Chief Scientist of Faraday Dynamics Co., Ltd. He received his B.Eng degree and M.Phil degree in electronic engineering department both from the Zhejiang University. He earned his Ph.D. degree in electronic engineering from the City University of Hong Kong. He joins Hangzhou Dianzi University in 2014. His research interests include Electronic Design Automation (EDA), Radio-Frequency (RF) Circuit, Computational Electromagnetics and Antennas. In 2017, as a co-founder, he founded Faraday Dynamics Co., Ltd., mainly engaged in the development of efficient EDA software.

PANEL DISCUSSION II

TOPIC	Global Market Trends and Future Directions in High-Speed Cables and Connectors
TIME	16:20 – 17:20, November 7th
VENUE	Room 4: XinHui Function Room @Level 2（2 楼新晖厅）
PANEL CHAIR	Fei Xue, Signal Integrity Engineer and Technical Lead, Intel
INVITED GUEST	Yang Yang, Server System Architect, IEIT SYSTEMS Xiaoquan Wang, CTO, Huaqin Technology Shiang Yao, Advanced Application and Development Specialist, 3M Terry Ke, Signal Integrity Supervisor, Amphenol AssembleTech Lei Deng, General Manager, Zhuhai LinkE Technology Co., Ltd. Xu Wang, Director, DeTooLIC Technology

KEY TOPICS INCLUDE:

- **Global Market Demands:** High-speed connectivity requirements for data centers, AI systems, and supercomputing infrastructure.
- **Technical Challenges and Standards Evolution:** Navigating the transition to higher-speed standards, such as PCIe 6.0, Ethernet 800G and beyond.
- **Innovative Solutions and Future Trends:** Exploring cutting-edge solutions and technological advancements to meet the industry's demands.

BIOS OF PANEL CHAIR

Fei Xue, Signal Integrity Engineer and Technical Lead, Intel

Harrison Xue Fei is a signal integrity engineer and technical lead in Intel since 2015, working on signal integrity of high-speed interconnects in server, storage and data center systems and client work station, desktop and laptop. He received his bachelor and master's degrees in University of Electronic Science and Technology of China (UESTC), Chengdu, China in 2002 and 2005 respectively.

BIOS OF INVITED PANELISTS

Yang Yang, Server System Architect, IEIT SYSTEMS

Yang Yang is server system architect from IEIT SYSTEMS, focusing on architecture design of AI server. He joined IEIT SYSTEMS in 2016 after graduating from Tsinghua University with master's degree. He participated in leading the architecture design of IEIT's multi generation AI flagship servers, he is now responsible for server platform technology planning and development.

Xiaoquan Wang, CTO, Huaqin Technology

Xiaoquan Wang is currently the CTO of Huaqin Data Division, and graduated from Nanjing University of Science and Technology with a master's degree in communication and information systems. He has 24 years of experience in the communications industry, having worked for well-known companies such as ZTE, Celestica and Huaqin Technology. Experienced in JDM and OEM services for North American customers, providing high-quality services to customers. He has led the design of the world's first backplaneless Orthogonal-Direct 100G switch, as well as all existing network 100G/200G/400G/800G high-speed switches developed for meta, AWS, and Google, and also led the design of 100G, 200G, 400G, and 800G high-speed switches for major Internet customers in China.

Shiang Yao, Advanced Application and Development Specialist, 3M

Yao Shiang, Advanced application and development Specialist on 3M high-speed signal interconnect solutions for data centers. Provide to users with the best application solutions based on signal integrity for products and the applications of interconnect architectures. Before joining 3M, worked in ZTE Shanghai R&D Center.

Terry Ke, Signal Integrity Supervisor, Amphenol AssembleTech

Terry Ke is a Signal Integrity Supervisor at Amphenol AssembleTech, where he leads SI support for high-speed cable assembly development. Graduated with a master degree from the University of Electronic Science and Technology of China, Terry has built a strong expertise in high-speed cable signal integrity and interconnect design. At Amphenol, he contributes to enhancing SI performance and closely working with industry partners on next-generation cabling applications.

Lei Deng, General Manager, Zhuhai LinkE Technology Co., Ltd.

Deng Lei is the General Manager of Zhuhai LinkE Technology Co., Ltd. He has over 15 years of R&D experience in high-speed interconnects, antenna technology and high-performance RF system design. Currently, he is leading the team to develop cutting-edge solutions for next-generation connectivity. He holds a bachelor's and master's degree from Huazhong University of Science and Technology.

Xu Wang, Director, DeTooLIC Technology

Xu Wang received the B.S and M.S degrees in electrical engineering from University of Electronic Science and Technology of China, Chengdu, China, in 2015 and 2018 separately. He received his Ph.D degree in electrical engineering from Missouri University of Science and Technology in 2023. He joined DeTooLIC Technology in 2024 and is currently the director of core technology department. His current research interests include the development of EDA tools for printed circuit boards and advanced packaging.

HOW TO GET TO THE INTERCONTINENTAL NINGBO

Taking the Airplane

Ningbo Lishe International Airport → InterContinental Ningbo

Once you get out of the luggage pickup area, take the Subway Line 2 first to the "Shiqi Station", then take Subway Line 5 to "Yuanshi Rd" (Exit F) to to arrive at InterContinental Ningbo. The Subway Ticket is 6 CNY. It can be purchased at the station using cash.

Another option is is taking Taxi, which costs around 70 CNY.

Taking the (High-speed)Train

Ningbo Station→ InterContinental Ningbo

Take Subway Line 2 from "Ningbo Railway Station" to "Sanguantang Station" then take Subway Line 5 to "Yuanshi Rd" (Exit F) to to arrive at InterContinental Ningbo. The Subway Ticket is 4 CNY. It can be purchased at the station using cash.

If you take Taxi, the estimated cost is around 50 CNY.

Driving by Yourself

Please search for "InterContinental Ningbo" in GPS. The navigation will plan your traffic route according to your current position.

Parking: InterContinental Ningbo parking lot with 700 underground spaces.

ACCOMMODATION

Special rates have been negotiated for the 2024 WAI in Ningbo attendees at InterContinental Ningbo.

If you need to book a room, please contact the hotel before November 1, 2024, quoting the name of the conference to make a reservation at the special rate.

Hotel Name：

InterContinental Ningbo
宁波洲际酒店

Hotel Address：

777 Xinhui Road, National High-tech Zone, Ningbo
宁波市鄞州区新晖路 777 号

Hotel Phone Number：

+86 574-89077777

Recommendations for other hotels:

Hotel Name：

UrCove by HYATT Ningbo International Exhibition Center
宁波国际会展中心逸扉酒店

Hotel Address：

1255, Heqing North Road, Yinzhou District, Ningbo
宁波市鄞州区河清北路 1255 弄

Hotel Phone Number：

会议协议价请咨询 17681995031/ 0574-8779 7888

Hotel Name：

Atour Hotel (Ningbo International Convention and Exhibition Center)
宁波国际会展中心亚朵酒店

Hotel Address：

No.724 Yangmuqi Road, Yinzhou District, Ningbo
宁波市鄞州区杨木碶路 **724** 号

Hotel Phone Number：

+86 574-27878899

Hotel Name：

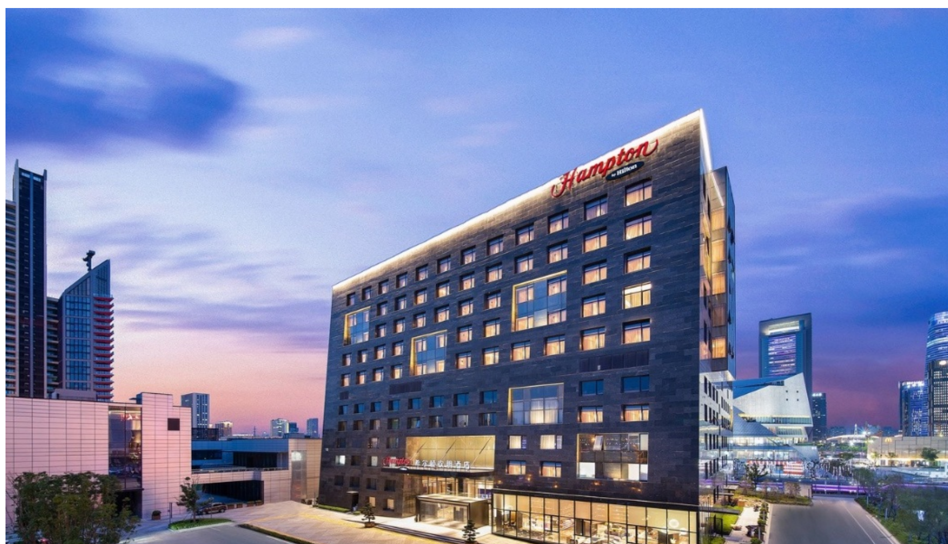
Hampton by Hilton Ningbo Eastern New Town
宁波东部新城希尔顿欢朋酒店

Hotel Address：

14 South District, Hongtai Plaza, Zhongshan East Rd, Yinzhou District, Ningbo
宁波市鄞州区中山东路宏泰广场（南区）**14** 号

Hotel Phone Number：

+86 574-27629888



ABOUT NINGBO

Ningbo, also known as Yong, is located halfway down the coastline of the Chinese mainland and to the south of the Yangtze River Delta. It is bordered by the natural bulwark of the Zhoushan Archipelago to the east, the city of Shaoxing to the west, the city of Shanghai to the north across the Hangzhou Bay, and the city of Taizhou and Sanmen Bay to the south.

The city's history can be traced back to the Hemudu Culture that originated 7,000 years ago. In the Xia and Shang Dynasties about 4,000 years ago, Ningbo was known as Yin. Later, in the Spring and Autumn Period (770-476 BC), it became part of the State of Yue. In the Qin Dynasty (221-206 BC), it encompassed Yin, Mao and Gouzhang, three areas under the Kuaiji Shire. In the Tang Dynasty (618-907 AD), it was named Mingzhou. In 821 AD, the local authority moved towards the junction of three local rivers and built city walls, marking the establishment of today's city. In 1381 AD, the city acquired its current name of Ningbo, or, literally, Calm Waves.