WAI 2025 Ningbo, China November 5 – 7, 2025

IEEE wai 2025

2025 International Workshop on
Advanced Interconnects
Ningbo, China

WAI 2025

November 5 – 7, 2025

Final Program

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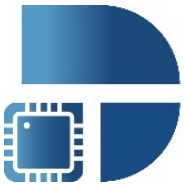

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INVITATION FROM THE GENERAL CHAIR

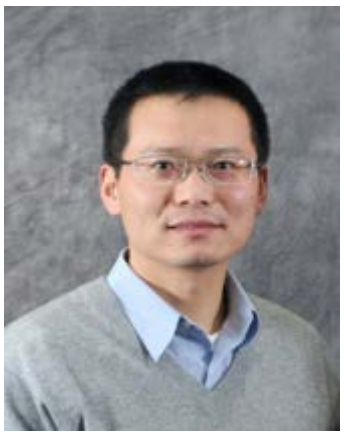
Dear Colleagues and Friends,

Welcome to WAI 2025! This is the second International Workshop on advanced interconnects. The scope of this workshop includes, but is not limited to, signal integrity and power integrity of an electronic system and its components, including advanced interconnects, integrated circuits, IC packages, printed circuit boards, cables, connectors, as well as other relevant electronic and microelectronic components, and signal integrity/ power integrity co-design.

WAI 2025 also welcomes all papers or presentations related but not limited to electromagnetic environments; interference control; EMC and EMI modeling; high power electromagnetics; EMC standards, methods of EMC measurements; computational electromagnetics and signal and power integrity, as applied or directly related to EMC problems; transmission lines; electrostatic discharge and lightning effects; EMC in wireless and optical technologies; EMC in printed circuit board and system design; radio-frequency interference problems; artificial intelligence-assisted EMC/SI/PI design methodologies.

We would like to express our thanks to our coorganizers, sponsors, contributors, and all of the attendees for your hard work and effort! Our best wishes are to all WAI 2025 attendees, and we hope all of you enjoy your time in Ningo and have a great time!

WAI 2025 General Chairs



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Er-Ping Li, IEEE Fellow

Qiushi Chair Professor, Zhejiang University

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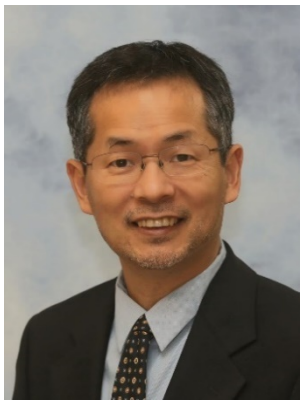

Xiaoning Ye, IEEE Fellow

Intel

Bo Pu

DeTooLIC Technology

Ling Zhang

Zhejiang University

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Jiang Xiao,
Keysight Technologies (China) Co., Ltd, China

GENERAL INFORMATION

REGISTRATION

Registration link:

please register an account at http://www.wai-emc.com/wai2025/registration.

Each participant or each presenting author must pay a non-refundable pre-registration fee. Only pre-registered and paid submissions before 26 October 2025 will be scheduled in the symposium program. Inclusion of the submissions in the final Technical Program (one-page abstracts only), and WAI Proceedings (one-page abstracts only) is guaranteed only after the pre-registration of the presenting author is completed.

Your pre-registration will be valid only if the payment is received timely. The pre-registration deadline is 26 October 2025. The on-site registration opportunity is for non-presenting authors only. The registration fee for your articles is non-refundable. The registration fee is the same for presenting authors and non-presenting authors.

Onsite Participants	Registration Fee
Student Full Price Ticket	RMB 1480 (USD 208)
Regular Full Price Ticket	RMB 2480 (USD 348)

CONFERENCE VENUE

HUALUXE® Ningbo Harbor City

The HUALUXE Hotel in Ningbo Port City is a new high-end five-star hotel brand under the InterContinental Hotels Group. Based on a globally renowned excellent management system, it is committed to providing you with a space that is close to nature and luxurious, bringing a new definition of Chinese hospitality to the Chinese people with "courtesy, respect, harmony, and expressiveness".

It is your ideal choice for business socializing and gathering with family and friends. The Huayi Hotel in Ningbo Port City understands the business and social needs of Chinese people. From relaxed meetings at the "Jumingyi" tea house, private banquets at the "Jushanyi" VIP world, to leisure and wellness at the Huayi Health Club, a series of public and private spaces fully meet the various business, social, and leisure entertainment needs of guests.

LOCATION MAP AROUND THE CONFERENCE VENUE

★HUALUXE® Ningbo Harbor City

Address: No. 1199 Changjiang Road, Beilun District, Ningbo City, Zhejiang Province

(+86 574 86799999)

Website: https://www.ihg.com.cn/hualuxe/hotels/cn/zh/ningbo/ngbul/hoteldetail#

REGISTRATION HOURS/FLOOR PLAN

Admission to all sessions and hosted functions requires an attendance identification. Please wear your name badge at all times.

Registration time

☐ November 4, Tuesday 16:00 - 19:00

☐ November 5, Wednesday 7:30 – 9:00

Registration Address

HUALUXE® Ningbo Harbor City

宁波港城华邑酒店

No. 1199 Changjiang Road, Beilun District, Ningbo City, Zhejiang Province

EXHIBITION HALL AND MEETING ROOMS

Opening Ceremony (开幕式及大会讲座)

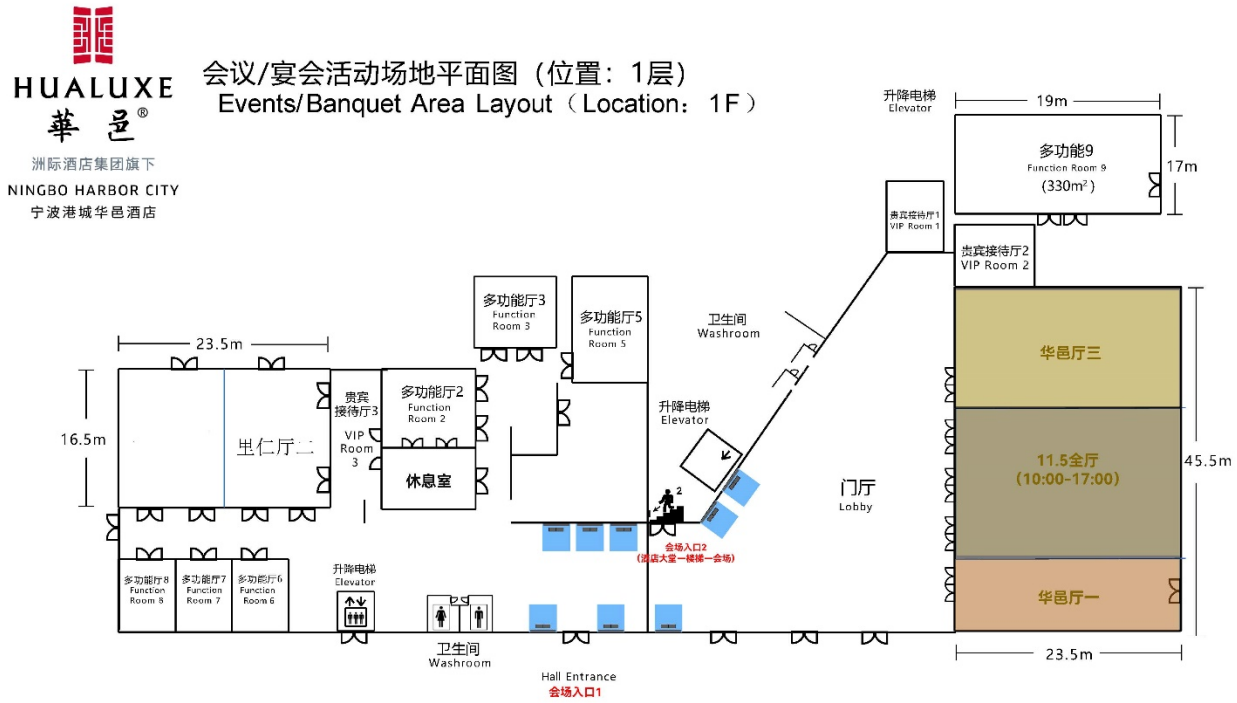
HUALUXE Hall @ 1F（1 楼华邑宴会厅）

Parallel Sessions (分会场)

Room 1: HUALUXE Hall 1 @ 1F（1 楼华邑厅一）

Room 2: HUALUXE Hall 3 @ 1F（1 楼华邑厅三）

Room 3: Liren Hall 2 @ 1F（1 楼里仁厅二）



PROGRAM OVERVIEW

Symposium Web: http://www.wai-emc.com/wai2025/

Symposium Hours

November 5, 2025, 8:30 – 17:30

November 6, 2025, 8:40 – 17:40

November 7, 2025, 8:40 – 12:00

November 5 – Wednesday

- ☐ Official Opening and Keynote Speeches
- ☐ Industry Plenary
- ☐ Technical Exhibition

November 6 – Thursday

- ☐ Oral Presentation
- ☐ Young Professionals Forum
- ☐ Technical Exhibition
- ☐ Banquet Dinner

November 7 – Friday

- ☐ IBIS Summit
- ☐ Oral Presentation
- ☐ Technical Exhibition

2025 International Workshop on Advanced Interconnects

November 5-7, 2025

Date	Time	Agenda
Nov. 5th	08:30-08:40	**Opening Ceremony**
	08:40-10:00	**Keynote Speeches**
	10:00-10:20	**Tea Break**
	10:20-12:20	**Keynote Speeches**
	12:20-14:00	**Lunch**
	14:00-15:30	**Industry Plenary**
	15:30-15:50	**Tea Break**
	15:50-17:20	**Industry Plenary**
	17:30	**Dinner (Buffet)**

2025 International Workshop on Advanced Interconnects
November 5-7, 2025

Date	Time	HUALUXE Hall 1（华邑厅一）	HUALUXE Hall 3（华邑厅三）	Liren Hall 2 （里仁厅二）
Nov. 6th	08:40-10:20	*[SS1] Signal and Power Integrity for High-Speed Interconnect Design*	*[SS3] Advance in Electromagnetism Simulation and Analysis Method*	*Industry Plenary (VII-VIII)*
	10:20-10:40	**Tea Break**		
	10:40-11:20	*[SS1] Signal and Power Integrity for High-Speed Interconnect Design*	*[SS3] Advance in Electromagnetism Simulation and Analysis Method*	*Panel Discussion I* *Addressing the Ever-Growing Challenges in High-Speed Interconnect Designs in the AI Era: EDA Perspectives*
	11:20-12:00	*[SS1] Signal and Power Integrity for High-Speed Interconnect Design*	*[SS3] Advance in Electromagnetism Simulation and Analysis Method*	
	12:00-13:20	**Lunch & Rest**		*Young Professionals Forum* （**Providing Lunch**）
		HUALUXE Hall 1（华邑厅一）	**HUALUXE Hall 3（华邑厅三）**	**Liren Hall 2（里仁厅二）**
	13:20-14:00	*[SS2] Recent Advances in EMI/EMC Techniques*	*[SS5]* **Machine Learning Based EMC/SI/PI Design**	*Panel Discussion II* *Data Center High-Speed Interconnect in the AI Era: Part I - Innovations in Materials and Manufacturing*
	14:00-14:40	*[SS2] Recent Advances in EMI/EMC Techniques*	*[SS5]* **Machine Learning Based EMC/SI/PI Design**	
	14:40-15:20	*[SS2] Recent Advances in EMI/EMC Techniques*	*[SS5]* **Machine Learning Based EMC/SI/PI Design**	*Panel Discussion III* *Data Center High-Speed Interconnect in the AI Era: Part II - Architecturing the Interconnect for the Future*
	15:20-15:40	**Tea Break**		
	15:40-16:40	*[SS4] Power Integrity Design Techniques*	*[SS6] Antenna Design Techniques*	*Panel Discussion IV* *Trends in Smart Devices and Challenges Related to Electromagnetic Interference in the AI Era*
	16:40-17:40	*[SS4] Power Integrity Design Techniques*	*[SS6] Antenna Design Techniques*	
	18:30	**Banquet Dinner**		
Nov. 7th	**Time**	**HUALUXE Hall 1（华邑厅一）**	**HUALUXE Hall 3（华邑厅三）**	**Liren Hall 2 （里仁厅二）**
	08:40-09:40	*[SS7] Electromagnetic Compatibility of Integrated Circuits and Components*	*[SS8] Advanced Signal Integrity Modeling, Design, and Testing Techniques*	*IBIS Summit*
	09:40-10:00	**Tea Break**		
	10:00-12:00	*[SS7] Electromagnetic Compatibility of Integrated Circuits and Components*	*[SS8] Advanced Signal Integrity Modeling, Design, and Testing Techniques*	*IBIS Summit*
	END			

KEYNOTE SPEECHES I

TITLE	**High-Speed Interconnect in Data Centers**
TIME	8:40 – 9:20, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	Xiaoning Ye, Intel

ABSTRACT

The data center is undergoing a profound shift from CPU-centric design to accelerated computing and generative-AI–centric architectures. The fundamental unit of compute is no longer a single server but a distributed system at rack and cluster scale. Achieving performance now hinges on massive data parallelism—and the interconnect has become the first-order constraint as system scale and bandwidth rise.

This speech traces the evolution of high-speed interconnects in modern data centers and explains why signal integrity now drives the ecosystem. We will also show how hardware-architecture innovations can relieve interconnect bottlenecks and unlock scalable performance.

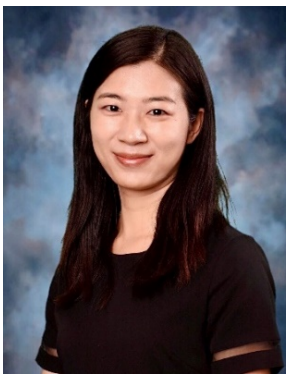
BIOGRAPHY

Dr. Xiaoning Ye is currently a Senior Principal Engineer at Data Center Group of Intel Corporation, specialized in high-speed interconnects. He received his Bachelor's and Master's degrees in electronics engineering from Tsinghua University, Beijing, China, in 1995 and 1997 respectively, and Ph.D. degree in electrical engineering from Missouri University of Science and Technology in 2000.

Dr. Ye published over 100 technical papers in IEEE and other technical journals and conferences, with over 3600 citations. He holds 20 patents and a few more applications in the areas of high-speed signaling. He also led the development of two industry standards on interconnect characterization: IEEE 370, and IPC test method 2.5.5.14. Dr. Ye is currently serving as Vice President of Technical Services for IEEE EMC Society. He was Chair of the IEEE EMC Society Technical Advisory Committee from 2017 to 2020, and has been an Associate Editor of IEEE Transactions on Electromagnetic Compatibility since 2016. Dr. Ye received Technical achievement award of IEEE EMC Society in 2015, and was elevated to IEEE fellow in 2021.

KEYNOTE SPEECHES II

TITLE	**Accelerating Innovation: AI-Driven Advances in Sigrity, Clarity, and Optimality**
TIME	9:20 – 10:00, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	Qin Liu, Cadence



ABSTRACT

With the electronic systems being more complex, the efficiency and accuracy requirement on design and simulation is becoming more and more demanding. At Cadence, we're meeting this challenge head-on by bringing AI and automation to every stage of design. Sigrity-APX, as an intelligent advanced IC Package Extractor, embeds machine learning models in many typical but challenging structures, such as vias, degassing hole planes, and traces with degassing hole planes. Clarity-PI is also launched as an AI accelerated Clarity extraction tool with faster, smarter and more stable solution, benefitting IC, interposer, and packaging extraction applications. Also, with new statistical functions and AI surrogate models, our advanced optimization engine allows user to explore the design space with higher efficiency. Furthermore, major break through is made in using generative AI beyond traditional optimization, we can now automate the entire workflow inside the design platform by creating new design from scratch, identifying critical regions, auto-cutting and extracting, and running targeted optimizations. AI algorithm, learning from Cadence's massive simulation datasets, predicts electromagnetic effects with high fidelity. This means fewer manual tweaks and more reliable results, accelerating the path to signoff.

BIOGRAPHY

Qin Liu is a Software Engineering Director in Sigrity R&D US Group at Cadence Design Systems, mainly focused on Clarity 3D full-wave electromagnetic software development. Dr. Liu has over 14 years' experience in developing advanced electromagnetic analysis and simulation methods. She received the B.Eng. degree in electronic engineering from the University of Science and Technology of China, Hefei, China, in 2011, and the Ph.D. degree in electrical and electronic engineering from The University of Hong Kong, Hong Kong, in 2015. From 2015 to 2018, she is a Post-Doctoral Fellow with The University of Hong Kong and a Postdoctoral Research Associate with the University of Illinois at Urbana Champaign. Since 2018, she has been working for Sigrity/Clarity R&D Group at Cadence Design System, San Jose, USA.

KEYNOTE SPEECHES III

TITLE	**High-Speed Interconnects in Semiconductor Systems: Where Physics Meets Performance**
TIME	10:20 – 11:00, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	En-xiao Liu, A*STAR

ABSTRACT

As semiconductor scaling is knocking on the door of the physical limits, interconnects open a new window into the spotlight of realizing system speed, bandwidth, energy, and reliability.

In this dense and deep connection era, multi-GHz signalling amplifies loss, crosstalk, and electrical and electromagnetic as well as multiphysics interactions across chip, package, and board hierarchies. Signal integrity, power integrity, and electromagnetic compatibility (SI/PI/EMC) can only be better achieved through multi-parameter and multi-objective early co-design and co-optimisation.

On one hand, advanced packaging, chiplets, and co-packaged optics create dense, multi-modal channels offering new hopes and new promises. On the other hand, AI and Machine learning (ML) are demanding even more from high-speed interconnects.

Can we leverage new physics, novel materials, heterogeneous architectures, AI/ML, and so on, to transform interconnects from passive links into active enablers of ultra-wide bandwidth, high-speed, energy-efficient, and robust systems?

BIOGRAPHY

En-Xiao Liu is currently Senior Principal Scientist and Deputy Department Director at A*STAR Institute of High Performance Computing. He is also an adjunct Associate Professor at the National University of Singapore. His research interests are in the areas of computational electromagnetics, high-speed electronics and packaging, electromagnetic compatibility (EMC), and AI/ML applications.

Dr. Liu received the team award of Singapore President's Technology Award (2019), ASEAN and IES Prestigious Engineering Achievement Award (2019), and the IEEE EMC Society Technical Achievement Award (2016). He was an IEEE EMC Society Distinguished Lecturer, the past Chair of the IEEE EMC Singapore Chapter, and TPC/General Chair for several international conferences. He is an Associate Editor of four IEEE journals (T-EMC, T-SPI, L-EMCPA, and T-CPMT). He co-edited the T-EMC (a) Special Section on Nature-Inspired Algorithms for EMC/SI/PI (2018) and (b) the Special Issue on AI/ML & Deep Learning for EMC (2024). He was a plenary speaker at the EMC Japan/APEMC Okinawa 2024 Symposium.

KEYNOTE SPEECHES IV

TITLE	**New Opportunity, New Journey**
TIME	11:00 – 11:40, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	Stanley Zheng, EDA²

ABSTRACT

With the rapid development of digitization, intelligence, and the great prospect of semiconductor industry, we are standing at an unprecedented node in the window where there are constrains of supply chain and technology bifurcations, this presents both new opportunities and unprecedented challenges, requiring industry and academia to jointly explore technological breakthrough with STCO Collaborative Development

BIOGRAPHY

Stanley Zheng graduated from the Department of Computer Science at Fudan University and holds an MBA from Macau University of Science and Technology. He has served as Senior Engineer at Inventec, Engineering Manager at Phoenix Technologies, Technical Support Manager/Strategy Director at Intel, and Director of Semiconductor Industry Development at Huawei. His work experience spans OS development, BIOS/EFI development, chip technical support, marketing, ecosystem promotion, IP strategy, 7nm chip product development, and industry development. He is the only person in Intel China ever served as a global chip leader. He currently serves as the Director of External Cooperation Committee and Chief of Standards at EDA².

KEYNOTE SPEECHES V

TITLE	**Multiphysics EDA: Advanced Computing beyond Simulation**
TIME	11:40 – 12:20, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	Qiwei Zhan, Zhejiang University

ABSTRACT

When discussing multiphysics modeling, the finite element method is one of the most widely used algorithms. However, especially for complex systems, there remains a significant gap between real-world requirements and current simulation capabilities. This challenge arises mainly due to extreme problem scales, unavoidable uncertainties, and prolonged simulation times.

Moreover, with IC design having entered the post-Moore's Law era, 3D chip integration has emerged as one of the most promising technologies. Yet, an effective EDA tool that incorporates coupled electromagnetic, thermodynamic, and fluid effects is still lacking.

These challenges motivate us to develop multiphysics EDA software, by integrating recent advances in computational methods and going beyond conventional FEM simulation. To be more specific, this talk will present interdisciplinary efforts, toward the systematic integration of CAD (mesh generation), CAE (unified discontinuous Galerkin methods), and CAM (data learning), empowered by the high-performance computing technology.

BIOGRAPHY

Qiwei Zhan received the B.S. degree in geophysics from the University of Science and Technology of China, Hefei, China, in 2013, and the M.S. degree in civil and environmental engineering (minor) and the Ph.D. degree in electrical and computer engineering from Duke University, Durham, NC, USA, in 2016 and 2019, respectively. From June 2019 to August 2020, he was a Peter O'Donnell Jr. Postdoctoral Fellow with the Oden Institute for Computational Engineering and Sciences, The University of Texas at Austin, Austin, TX, USA. Since September 2020, he has been a Tenure-Track Professor and a Ph.D. Supervisor with the College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China. His research interests include multiphysics modeling, high-performance computing, uncertainty quantification, inverse problems, and scientific machine learning.

INDUSTRY PLENARY I

TITLE	**China's RISC-V High-Performance Computing: Exploration from Self-Developed IP to Ecosystem Construction**
TIME	14:00 – 14:30, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	Qingyuan Ren, RiVAI

ABSTRACT

This speech examines RISC-V's disruptive role in high-performance computing (HPC), highlighting global momentum and China's accelerated progress through strategic policy support. One of this evolution is RiVAI Technologies' Lingyu Processor—featuring a dual-core architecture, self-developed Core & NoC IP, and enterprise-grade RAS for data-center reliability. The speech further demonstrates a full-stack RISC-V HPC solution encompassing hardware co-developed with top OEMs and domestic software partners. Empowered by a robust ecosystem, RISC-V is advancing scenario-specific deployments (AI inference, industrial HPC) toward a multi-billion-dollar market, redefining next-generation computing infrastructure.

BIOGRAPHY

Mr. Ren Qingyuan graduated from Duke University and the University of Washington in the United States and previously held positions at leading industry companies such as Lenovo. In 2023, he joined RiVAI Technologies as Business Vice President, where he oversees the company's commercial and marketing operations.

INDUSTRY PLENARY II

TITLE	**Testing Solutions for Ultra-High-Speed Products ----- Signal Integrity Testing for Passive Components**
TIME	14:30 – 15:00, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	Xiangyang Ma, Dloorplf

ABSTRACT

With the advent of generative AI, artificial intelligence has achieved leapfrog development in the 2020s, placing higher demands on hardware in terms of computing power, storage, and data transmission—requiring faster iteration, higher speeds, and quicker responses. In an increasingly demanding market, how can we grasp the right direction and solutions for product R&D and manufacturing to create better products? Share Dloorplf's solutions.

BIOGRAPHY

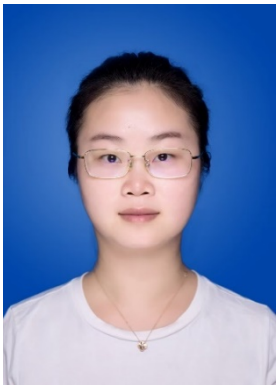
Industry-leading expert developers: Proficient in high-frequency and millimeter-wave communications, with 24 years of industry experience. Expertise in network analysis, S-parameters, DCA, RF SI, and related systems and development technologies.

•Possesses extensive project development management experience, having led full-cycle development and team management for 10G/40G Ethernet, 100G SR4/LR4, wireless modules, Apple millimeter-wave matrix, and 400G/800G optical transmission test systems. Expertise spans optical transmission, high-frequency transmission and integrity, and wireless signal system processing.

•Proficient in both software and hardware: Expertise in C/VB language interface systems, mastery of high-frequency PCB design and signal processing.

INDUSTRY PLENARY III

TITLE	**Development Status of InP and CMOS Heterogeneous Integration Technology**
TIME	15:00 – 15:30, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	Rong Chen, Microsystem Integration Group at the National Laboratory of Integrated Circuits and Microsystems, CETC



ABSTRACT:

InP and CMOS are two distinct semiconductor materials with its unique advantages and limitations. InP materials feature high electron mobility and high cutoff frequency, making them suitable for high-frequency and optoelectronic device fabrication. CMOS materials offer high electron mobility and high integration density, making them ideal for digital integrated circuits. To achieve frequencies of >100 GHz, the heterogeneous integration of InP and CMOS can offer superior performance and application value. However, there are several technical challenges in the integration process： particularly concerning material compatibility, device interoperability, and manufacturing processes. As a result, the heterogeneous integration of InP and CMOS has become a key area of research in recent years. This paper analyzes the development status of InP and CMOS heterogeneous integration technology, examines the main challenges currently faced by the technology, and explores future development directions, providing strong support for high-frequency (>100 GHz) wireless communications, radar imaging, and other high-performance applications.

BIOGRAPHY

Rong chen is an advanced packaging expert at CETC Chip Institute and Head of the Microsystem Integration Group at the National Laboratory of Integrated Circuits and Microsystems. She has led or participated in over ten national and ministerial-level key projects. Her current research is dedicated to 2.5D packaging and Chiplet technologies for high-speed, high-precision mixed-signal circuits, with over 10 publications and 3 patents.

INDUSTRY PLENARY IV

TITLE	**Research on Simulation and Testing of Signal Integrity and Power Integrity**
TIME	15:50 – 16:20, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	Jianguo Zhang, Sanechips Technology Co., Ltd.

ABSTRACT

This article mainly introduces the work on SI fitting of encapsulated high-speed ABF materials and the simulation study on PI noise consistency. It focuses on how, during the material fitting process, the return loss SDD11 can be kept within an error of less than 1 dB, and how the PI noise error can be maintained within 5%.

BIOGRAPHY

Master's degree in Electromagnetic Field from University of Electronic Science and Technology of China. Joined ZTE Microelectronics in 2021 as a Level 5 Technical Expert in the SIPI field, responsible for SIPI simulation technology and methodology for the packaging team, and serves as the head of the Chengdu Packaging Department.

Previously worked at several well-known companies in the industry, offers basic SI simulation courses. Personal public account: <High-Speed Circuits and Signal Integrity>， @Half a RF Engineer

INDUSTRY PLENARY V

TITLE	**Speed Up 112/224G Design with Clarity 3D Solver and Optimality Explorer**
TIME	16:20 – 16:50, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	Kezhou Li, Cadence

ABSTRACT:

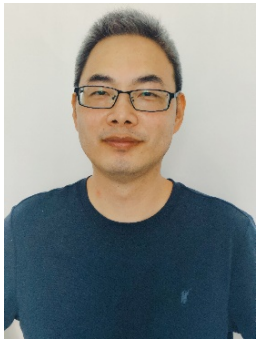
As cloud applications and large language models like GPT become increasingly widespread, network providers are compelled to upgrade transmission bandwidth, which requires advanced SerDes technology. The OIF organization initiated the CEI-224G project in 2020; if the 112G SerDes PAM4 scheme is adopted, the fundamental frequency reaches 56GHz, posing significant challenges for high-speed signal transmission across entire systems. Conventional design and simulation workflows often optimize individual components, but robust SerDes development at 112/224Gbps demands entire channel path analysis and system-level design optimization, accounting for all components' interactions. This presentation introduces how Cadence Clarity 3D Solver and Optimality Explorer efficiently enable global design and optimization for 112/224Gbps SerDes.

BIOGRAPHY

Kezhou Li is a seasoned expert in electromagnetic simulation with over 15 years of experience. As a Director in Cadence's System Design and Analysis (SDA) Group, Kezhou leads the Product Engineering and Verification Team in China. He has witnessed Cadence's remarkable growth in the system simulation domain and plays a key role in shaping the roadmap for flagship tools in electronic simulation.

INDUSTRY PLENARY VI

TITLE	**Evaluation and Solutions for Electrothermal and Mechanical Stress Challenges in Large-Chip Applications**
TIME	16:50 – 17:20, November 5th
VENUE	HUALUXE Hall @ 1F（1 楼华邑宴会厅）
SPEAKER	Yi Chen, ZTE Corporation



ABSTRACT

With increasing chip size and power consumption, the electrical, thermal, and mechanical stress issues in chip applications are becoming deeply intertwined. This article introduces evaluation methods and corresponding solutions to address these electro-thermal-stress challenges.

BIOGRAPHY

Earned a Master's degree from Harbin Institute of Technology. Joined ZTE Corporation in 2007 and possesses 20 years of experience in hardware development. Currently serving as the principal leader of the SI/PI team for wireless digital hardware and server products, with focused expertise in SerDes/DDR high-speed interface hardware design, evaluation, as well as SI/PI research related to chip packaging solutions and BBU/server architecture.

INDUSTRY PLENARY VII

TITLE	**Electromagnetic Compatibility (EMC) Simulation Applications in a Full-Vehicle Environment**
TIME	8:40 – 9:10, November 6th
VENUE	Liren Hall 2 @ 1F（1 楼里仁厅二）
SPEAKER	Ming Zhou, Simulia CST

ABSTRACT

Electromagnetic Compatibility (EMC) Simulation Applications in a Full-Vehicle Environment. Abstract: Full-vehicle EMC simulation faces significant challenges, including numerous EMI noise sources, complex noise propagation paths, difficulties in model simplification, and the inability to easily create simulation models from within components. CST Studio Suite has a wealth of application cases in full-vehicle EMC simulation, covering simulations for Conducted Emissions (CE), Radiated Emissions (RE), and Bulk Current Injection (BCI).

BIOGRAPHY

Zhou Ming earned his Master of Engineering degree from Harbin Institute of Technology. He has long specialized in electromagnetic field simulation technology research and possesses rich engineering application experience, providing CST simulation guidance and technical support to major clients in the high-tech and automotive industries.

INDUSTRY PLENARY VIII

TITLE	**EMI Mechanisms, Parameters, and Measurements in High-Speed Systems: A Case Study of a Multi-Line Card Switch**
TIME	9:10 – 9:40, November 6th
VENUE	Liren Hall 2 @ 1F（1 楼里仁厅二）
SPEAKER	Caijun Zhao, Huawei Technologies Co., Ltd.

ABSTRACT

Taking a switch with multiple line cards as an example, this report systematically expounds on the electromagnetic interference (EMI) mechanism of high-speed systems, the EMI parameters of high-speed components, and their measurement methods. The EMI of high-speed systems is produced by high-speed components, such as chips, connectors, and optical modules. While a chip radiates emission, it can also excite connectors' radiation. The radiation of optical modules is divided into two parts according to where its radiation is from. The EMI of all high-speed components can be characterized in accordance with standard methods. Finally, the calculation and measurement results for some systems are given. The maximum discrepancy does not exceed 5 dB.

BIOGRAPHY

Dr. Caijun Zhao is currently serving as an Assistant Principal Expert at the 2012 Labs of Huawei Technologies Co., Ltd., focused on electromagnetics and protection. He received his Ph.D. degree in mechatronic engineering from Southeast University, Nanjing, China, in 2011. Dr. Zhao is engaged in the research and application of electromagnetics and protection technologies for communication systems, such as electromagnetic interference (EMI) of high-speed chips and systems, lightning and electrostatic protection, measurement of electromagnetic parameters of materials, and electromagnetic compatibility (EMC) testing.

Technical Sessions – Thursday, NOVEMBER 6, 2025

Room	*HUALUXE Hall 1*		*HUALUXE Hall 3*		*Liren Hall 2*
	SS1: Signal and Power Integrity for High-Speed Interconnect Design		**SS3: Advance in Electromagnetism Simulation and Analysis Method**		**Industry Plenary**
SESSION CHAIRS	***Francesco de Paulis,*** *University of L'Aquila, Italy*	***Seungyoung Ahn,*** *Korea Advanced Institute of Science and Technology, Korea (South)*	***Xiong Chen,*** *Xi'an Jiaotong University, China*	***Xiuqin Chu,*** *Xidian University, China*	***Ling Zhang,*** *Zhejiang University, China*
08:40-09:00	LPDDR SIPI Design Experience in Automotive Cockpit SoC and Microwave Nondestructive Evaluation Technique for Packaging Material (***Invited***) *(Chao Liu, Southeast University, China)*		Exploring Advanced Packaging in 2.5D/3D IC EDA: A Unified Platform for Backend Physical Design Simulation and Verification (***Invited***) *(Yi Zhao, Zhuhai Silicon Chip Technology Ltd., China)*		Electromagnetic Compatibility (EMC) Simulation Applications in a Full-Vehicle Environment *（Ming Zhou, CHINA SIMULIA Electromagnetics Industry Process Senior Consultant）*
09:00-09:20	Design and Analysis of Perforated Ground Plane for Mode Conversion Mitigation in High-Speed Differential Channel of Die-to-Die Interface *(Hyunwoo Kim, Korea Advanced Institute of Science and Technology University, Korea (South))*		Fast EM Algorithms for Interconnects in 2.5D/3D Integrated Circuits ***(Invited)*** *(Shunchuan Yang, Beihang University, China)*		EMI Mechanisms, Parameters, and Measurements in High-Speed Systems: A Case Study of a Multi-Line Card Switch *(Caijun Zhao, Huawei Technologies Co., Ltd.)*
09:20-09:40	Comparative Study of Delay Extraction Methods of Long SFP+ High Speed Cables for Signal Integrity Applications *(John Xiao, Keysight, China & Keysight (China), China)*		Physics-Constrained Differential Evolution for Continuous Decoupling Capacitor Placement and Orientation Optimization *(Li Jiang, Zhejiang University, China)*		
09:40-10:00	Modeling Capacitive-Loaded Unintentional Stubs in High-Speed Channels (*Nicolò Vicari, University of L'Aquila, Italy*)		Dielectric Reconfigurable S-band Planar Phase Shifter *(Yichen Liu, Xi'an Jiaotong University, China)*		***Panel Discussion***
10:00-10:20	Random Jitter Amplification Coefficient Calculation for NRZ PRBS Signal *(Tao Wei, Xidian University, China)*		Analysis of the Influence of Three - Proof Coating on the High - Speed Signal Transmission Performance of Embedded Computers *(Zichun Zhang, Xi'an Aeronautics Computing Technique Research Institute, China)*		
10:40-11:00	Comprehensive Measurement-to-Simulation Methodology for Better Gigabit Interconnect Evaluation and Exploration *(Tim Wang Lee, Keysight Technologies, USA)*		An Equation Based Solver for High-Speed Differential Pairs Affected by Fiber Weave Effect *(Kai Li, Cisco Systems, Inc., China)*		***Panel Discussion I*** Addressing the Ever-Growing Challenges in High-Speed Interconnect Designs in the AI Era: EDA Perspectives
11:00-11:20	Design Challenges and Optimization Strategies for High-Speed Connector Test Fixtures *(Lei Deng, LinkE Technologies, China)*		An Integrated Simulation Software for Component EMC Design and Analysis *(Jianhao Ge, Beihang University, China)*		
11:20-11:40	High-Order Markov Modeling of DFE Error Propagation Under Residual ISI Using SBR-Derived Transitions *(Yuhao Huang, Xidian University, China)*		Liquid Gated Network-Based Signal Integrity Analysis for High-Speed Links *(Yuxiang Tian, Zhejiang University, China)*		
11:40-12:00	Research on Physical Layer Signal Automated Testing Technology for Non-Standard Hardware Products *(Chuangye Guo, Avic Xi'an Aeronautics Computing Technique Research Institute, China)*		Addressing the Radio Frequency Interference Problem Through Characteristic Mode Analysis *(Xu Wang, Zhejiang University, China)*		

Room	*HUALUXE Hall 1*		*HUALUXE Hall 3*		*Liren Hall 2*
	SS2: Recent Advances in EMI/EMC		**SS5: AI/ML based EMC/SI/PI Design**		**Panel Discussion**
SESSION CHAIRS	***Si-Ping Gao,*** *Nanjing University of Aeronautics and Astronautics, China*	***Huapeng Zhao,*** *University of Electronic Science and Technology of China, China*	***Dawei Wang,*** *Hangzhou Dianzi University, China*	***Xiaohe Chen,*** *China University of Petroleum, China*	***Bo Pu,*** *DeTooLIC Ltd. Technology, China*
13:20-13:40	Recent Progress of Fast Direct Partial Element Equivalent Circuit Method (***Invited***) *(Huapeng Zhao, University of Electronic Science and Technology of China, China)*		Application of Optimization Algorithms in Channel Signal Integrity Design *(Qihang Shang, DeTooLIC Ltd. Technology, China)*		***Panel Discussion II*** Data Center High-Speed Interconnect in the AI Era: Part I - Innovations in Materials and Manufacturing
13:40-14:00	Suppressing Evanescent Wave Coupling Using Anisotropic Metasurface in Small Cavity Circuit (***Invited***) *(Da Yi, Chongqing University, China)*		High-Speed Link Surrogate Modeling Based on Multimodal Machine Learning *(XiaoYang Wu, Hang Zhou Dian Zi University, China))*		
14: 00-14:20	Recent Advances in YIG-Based Frequency Selective Limiters *(Si-Ping Gao, Nanjing University of Aeronautics and Astronautics, China)*		An Efficient Thermal-Aware Placement Method for Chiplet-Oriented Integrated Microsystems *(Peng Zhang, Hangzhou Dianzi University, China)*		
14:20-14:40	A Reconfigurable Dual-Polarized Metasurface Capable of Switching Between Absorption and Transmission Modes *(Pei Zhang, Zhejiang University, China)*		Machine Learning-Assisted S-Parameter Frequency-Domain Extrapolation Method *(Fei Zhou, Hangzhou Dianzi University, China)*		***Panel Discussion III*** Data Center High-Speed Interconnect in the AI Era: Part II - Architecturing the Interconnect for the Future
14:40-15:00	Magnetic and Electric Shielding Effectiveness Measurement of System-in-Package *(Di Wang, Zhejiang University, China)*		DNN-Based Prediction of Frequency-Dependent RLGC Parameters for Transmission Lines *(Jiaqi He, Xidian University, China)*		
15:00-15:20	S-Band Tunable Impedance Matching Network with Varactor Diodes *(Zhou Han, Xi'an Jiaotong University, China)*		PCB Stack-Up Recognition Using LLMs *(Jie Li, Southwest University of Science and Technology, China)*		
	SS4: Power Integrity Design Techniques		**SS6: Antenna Design Techniques**		
SESSION CHAIR	***Jun Wang,*** *Xidian University, China*	***Xinglin Sun,*** *Zhejiang University, China*	***Guangxiao Luo,*** *North China Electric Power University (Baoding), China*	***Syed Muzahir Abbas,*** *Macquarie University, Australia*	
15:40-16:00	A Hierarchical Optimization and Learning Framework for Broadband MLCC Equivalent-Circuit Modeling *(Yongjie Chen, Zhejiang University, China)*		An Efficient 2D/3D Mesh-Coupled Electro-Thermal Co-Simulation Method for Large-Scale Integrated Millimeter-Wave Phased Arrays *(Xinhong Xie, Donghai Laboratory, China)*		***Panel Discussion IV*** Trends in Smart Devices and Challenges Related to Electromagnetic Interference in the AI Era
16:00-16:20	Calculation Method for Statistical Distribution of Power Supply Noise in Chip-Package-PCB Co-Design *(Yuhuan Luo, Xi'an University of Posts and Telecommunications, China)*		Computational Modeling of a Microstrip Antenna and Measurements with a Nano VNA *(Kenedy Marconi Geraldo Santos, IFBA, Brazil)*		
16:20-16:40	Multi-Objective Decap Optimization Based on Non-Dominated Sorting Genetic Algorithm *(Keyi Ding, Zhejiang University, China)*		CPW Antenna for Satellite Earth Mapping and Radiolocation Systems *(Marcelo B Perotoni, UFABC, Brazil)*		
16:40-17:00	Overestimation of Inductance in PDN Modeling: A Study on MLCC Models *(Cailiang Fu, Southwest University of Science and Technology, China)*		Dual Wideband Metasurface Based Linear to Circular Polarizer for Transmission Mode *(Fatima Ghulam, Zhejiang Normal University, China)*		
17:00-17:20	Attention-Guided Reinforcement-Genetic Optimizer: Fast PDN Impedance Prediction and Decoupling Capacitor Design for Power Integrity *(Qiyu Jiang, Beijing University of Posts and Telecommunications, China)*		Spiral Blade-Inspired Polarization-Insensitive X-Band FSS for EMI Shielding Applications *(Saad Hassan Kiani, Universiti Teknikal malaysia, Melaka, Malaysia)*		
17:20-17:40	Simulation and Test of 112Gbps SerDes Power Noise *(Lingyun Liu, SANECHIPS Technology CO. LTD, China)*		Calibration of Simple Transient Electric Field Probe and Circuit-Based Waveform Reconstruction *(Guangxiao Luo, North China Electric Power University (Baoding), China)*		

Technical Sessions – Friday, NOVEMBER 7, 2025

Rooms	*HUALUXE Hall 1*		*HUALUXE Hall 3*		*Liren Hall 2*	
	SS7: Electromagnetic Compatibility of Integrated Circuits and Components		**SS8: Advanced SI Modeling, Design, and Testing Techniques**		**IBIS Summit**	
SESSION CHAIRS	***Fayu Wan,*** *Nanjing University of Information Science and Technology, China*	***Anfeng Huang,*** *DeTooLIC Ltd. Technology, China*	***Lei Deng***, *LinkE Technologies, China*	***Si-Ping Gao,*** *Nanjing University of Aeronautics and Astronautics, China*	***Randy Wolff,*** *Siemens EDA, USA*	***Ling Zhang,*** *Zhejiang University, China*
08:40-09:00	From Standard Interpretation to Testing Practice: Exploring the Path to High-Quality CDM Testing (***Invited***) *(Bingsheng Gao, ESDEMC, China)*		A de-Embedding Method for High-Speed Single-Ended Signals with Three-Port Test Fixture *(Rui Miao, Xidian University, China)*		IBIS Chair's Report (*Doug Burns, SI-Clarity, USA)*	
09:00-09:20	Research on the Influence of Signal Integrity of the Test Board on the CAN Transceivers Electromagnetic Interference Test *(Qi Li, National New Energy Vehicles Technology Innovation Center, China)*		A Novel Method for Calculating Crosstalk de-Embedding Transfer Function in High-Speed Link (*Rui Chen, Xidian University, China*)		IBIS Power Integrity Introduction *(Walter Katz, MathWorks and Arpad Muranyi, Siemens EDA, USA)*	
09:20-09:40	A Broadband Miniature TEM Cell for IC EMC Measurement over 8 GHz *(Chenghao Lan, Jimei University, China)*		Novel Methodology for Electrical Performance Characterization of High-Speed Raw Cables Under Thermal Stress *(Jimmy Hsu, Intel, Taiwan)*		IBIS Interconnect Task Group Update: Touchstone 3.0 Features & Progress *(Michael Mirmak, Intel, USA)*	
10:00-10:20	Comparative Study of BSS Algorithms for Noise Source Localization *(Hailing Zhao, Southwest University of Science and Technology, China)*		Delay Matters: Enhancing S-Parameter Macromodeling Accuracy *(Chenxi Liu, DeTooLIC Ltd. Technology, China)*		IBIS 8.0: Specification and Parser Introduction *(Randy Wolff, Siemens EDA, USA)*	
10:20-10:40	Exploration of the Relationship Between Copper Foil Microstructure and Etching Behavior on PCB Signal Integrity *(Changdong Gu, Zhejiang Huanergy, China)*		Connectors for 400 Gbps-per-Lane Links: Challenges and Design Directions *(Lei Deng, LinkE Technologies, China)*		Efficient Time-Domain Noise Analysis Method *(Xiuqin Chu, Xidian University, China)*	
10:40-11:00	Charged Device Model Electrostatic Discharge Sensitivity Tester Based on 3D Vision *(Minfeng Xia, Nanjing University of Information Science and Technology, China)*		Twinax Cables at 448 Gb/s: Challenges and Solutions *(Lei Deng, LinkE Technologies, China)*		Conquer MIPI C-PHY Simulation Challenge *(Xiuguo Jiang, Keysight Technologies, China)*	
11:00-11:20	Integrated Coaxial Resonator for Reconfigurable Passive Intermodulation Testing *(Min Liang, Xi'an Jiaotong University, China)*		2.4 GHz Wideband Tunable Impedance Matching Network *(Bin Han, Xi'an Jiaotong University, China)*		A Novel Physics-Assisted Genetic Algorithm for Decap Optimization *(Ling Zhang, Zhejiang University, China)*	
11:20-11:40	Tunable Phase Shifter Using Monolithic Sliding Triple-Line Structure *(Yuhan Liu, Xi'an Jiaotong University, China)*		Implementation of an Adaptive DFE Algorithm *(Wenbo Zhang, Avic Xi'an Aeronautics Computing Technique Research Institute, China)*			
11:40-12:00	A Method for Generating Approximately Non-Diffracting Möbius Rings *(Yueyi Yuan, Harbin Institute of Technology, China)*		Research on GMSL Testing Technology in Multi-Physical Field Environments *(Yuxu Huo, Avic Xi'an Aeronautics Computing Technique Research Institute, China)*			

OVERVIEW OF SESSIONS I

SESSIONS	[SS1] Signal and Power Integrity for High-Speed Interconnect Design
VENUE	HUALUXE Hall 1
TIME	08:40-12:00 November 6th
SESSION CHAIR	Francesco de Paulis, University of L'Aquila, Italy Seungyoung Ahn, Korea Advanced Institute of Science and Technology, Korea (South)
TECHNICAL TALKS	**LPDDR SIPI Design Experience in Automotive Cockpit SoC and Microwave Nondestructive Evaluation Technique for Packaging Material （Invited）** *Chao Liu, Southeast University, China* **Design and Analysis of Perforated Ground Plane for Mode Conversion Mitigation in High-Speed Differential Channel of Die-to-Die Interface** *Hyunwoo Kim (Korea Advanced Institute of Science and Technology University, Korea (South)); Seunghun Ryu (Korea Advanced Institute Science and Technology (KAIST), Korea (South)); Sanguk Lee, Seonghi Lee, Dongryul Park, Jinwook Lee and Seungyoung Ahn (Korea Advanced Institute of Science and Technology, Korea (South))* **Comparative Study of Delay Extraction Methods of Long SFP+ High Speed Cables for Signal Integrity Applications** *John Xiao (Keysight, China & Keysight (China), China)* **Modeling Capacitive-Loaded Unintentional Stubs in High-Speed Channels** *Nicolò Vicari (University of L'Aquila, Italy); Rick Rabinovich (Keysight Technologies, USA); Samuel Kocsis (Amphenol, USA); Kevin Mammenga (Wilder Technologies, USA); Gang Zhang (Harbin Institute of Technology, China); Carlo Olivieri and Francesco de Paulis (University of L'Aquila, Italy)* **Random Jitter Amplification Coefficient Calculation for NRZ PRBS Signal** *Tao Wei, Yuhao Huang and Haiyue Yuan (Xidian University, China); Yuhuan Luo (Xi'an University of Posts and Telecommunications, Xi' an, Shaanxi, China); Jun Wang (Xidian University, China); Xiuqin Chu (Xidian University, China)* **Comprehensive Measurement-to-Simulation Methodology for Better Gigabit Interconnect Evaluation and Exploration** *Tim Wang Lee, Mike Resso and JiWei Du (Keysight Technologies, USA)* **Design Challenges and Optimization Strategies for High-Speed Connector Test Fixtures** *Lei Deng (LinkE Technologies, China)* **High-Order Markov Modeling of DFE Error Propagation Under Residual ISI Using SBR-Derived Transitions** *Yuhao Huang, Tao Wei and Haiyue Yuan (Xidian University, China); Yuhuan Luo (Xi'an University of Posts and Telecommunications, Xi' an, Shaanxi, China); Jun Wang (Xidian University, China); Xiuqin Chu (Xidian University, China)* **Research on Physical Layer Signal Automated Testing Technology for Non-Standard Hardware Products** *Chuangye Guo, Yuxu Huo and Chaoyu La (AVIC Xi'an Aeronautics Computing Technique Research Institute, China); Tingting Liu (Avic Xi'an Aeronautics Computing Technique Research Institute, China)*

TITLE	**LPDDR SIPI Design Experience in Automotive Cockpit SoC and Microwave Nondestructive Evaluation Technique for Packaging Material (Invited)**
TIME	08:40-09:00 November 6th
VENUE	HUALUXE Hall 1
AUTHOR	Chao Liu (Southeast University, China)

ABSTRACT

Low Power Double Data Rate (LPDDR) memory has been widely used in many fields including electric vehicles, and its communication with cockpit SoC chips provides fundamental computing power support for in-vehicle information systems. The continuous increase in LPDDR transmission rates presents challenges in signal and power integrity (SIPI) for the interconnect design. This talk will introduce some representative SIPI issues met in LPDDR interconnect design towards advanced cockpit SoC, the analysis methodologies, and the layout and routing design driven by SIPI in the context of high computational power. Meanwhile, the structure integrity of the packaging material also affects signal integrity, flaws under a transmission line such as voids, cracks, and the nonideal permittivity distribution due to manufacturing issues or aging need to be inspected, this talk will introduce a microwave nondestructive evaluation technique capable of providing real-time three-dimensional and high-resolution images for the packaging materials. As a result, a function and structure co-analysis technique for exploring reliability limit and achieving long-term signal integrity is being developed to optimize the signoff procedure.

BIOGRAPHY

Chao Liu received his B.S. degree in electronic information engineering from Xidian University, Xi'an, China, in 2014, the M.S. degree in electromagnetic field and microwave technology from Southeast University, Nanjing, China, in 2017, and the Ph. D. degree in electrical engineering from Iowa State University (ISU), Ames, IA, USA, in 2021. Currently, he is the Young Chief Professor in the School of Information Science and Engineering, Southeast University. He was a Ph.D. student in electrical engineering at Missouri University of Science and Technology, Rolla, MO, USA, from 2018 to 2019, prior to transferring to ISU. After his graduation, he joined Qualcomm Technologies, Inc., San Diego, CA, USA, as a Senior Engineer, in 2022, working on signal and power integrity. In late 2023, he started his role as an Assistant Professor in Southeast University, Nanjing, China, affiliated with the School of Information Science and Engineering, and also affiliated with the State Key Laboratory of Millimeter Waves. He was promoted to a full professor by the end of 2024. His research interests primarily focus on signal and power integrity, microwave and millimeter-wave nondestructive evaluation.

Dr. Liu is a member of IEEE-Eta Kappa Nu (IEEE-HKN). He was a recipient of the Best Student Paper Award (Second Place) from the 2020 Annual Meeting and Symposium of Antenna Measurement Techniques Association (AMTA), the R. Bruce Thompson Graduate Fellowship from the Center for Nondestructive Evaluation, ISU, in both 2020 and 2021, and the Best Paper Finalists from 2022 IEEE International Instrumentation and Measurement Technology Conference (I2MTC).

TITLE	**Design and Analysis of Perforated Ground Plane for Mode Conversion Mitigation in High-Speed Differential Channel of Die-to-Die Interface**
TIME	09:00-09:20 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Hyunwoo Kim (Korea Advanced Institute of Science and Technology University, Korea (South)); Seunghun Ryu (Korea Advanced Institute Science and Technology (KAIST), Korea (South)); Sanguk Lee, Seonghi Lee, Dongryul Park, Jinwook Lee and Seungyoung Ahn (Korea Advanced Institute of Science and Technology, Korea (South))

ABSTRACT
In this paper, we present a perforated ground plane design that effectively mitigates mode conversion in highspeed differential channels. The proposed design employs perforated ground unit cells (PGUCs) with symmetric geometry and periodic arrangement to achieve uniform return current distribution. Mode conversion analysis using UCIe die-to-die interfaces demonstrates consistent performance around -70 dB across different channel configurations, compared to conventional designs varying from -68.5 dB to -43 dB depending on channel placement.

TITLE	**Comparative Study of Delay Extraction Methods of Long SFP+ High Speed Cables for Signal Integrity Applications**
TIME	09:20-09:40 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	John Xiao (Keysight, China & Keysight (China), China)

ABSTRACT
This paper presents a comparative study of three time delay extraction schemes for the long SFP+ high speed copper cables modelling. First one is Hilbert transform method based on a direct linear system delay calculation. Second one is Gabor transform method based on a very intuitive wavelet transform approach. Finally, we consider an algorithm based on the quasi-compact support wavelet, Morlet wavelet transform, both in time and frequency domain. These three methods are applied to time delay extraction of five long SFP+ cables after a simple example validation and comparison. The Morlet wavelet transform shows the best one for SFP+ cable delay extraction.

TITLE	**Modeling Capacitive-Loaded Unintentional Stubs in High-Speed Channels**
TIME	09:40-10:00 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Nicolò Vicari (University of L'Aquila, Italy); Rick Rabinovich (Keysight Technologies, USA); Samuel Kocsis (Amphenol, USA); Kevin Mammenga (Wilder Technologies, USA); Gang Zhang (Harbin Institute of Technology, China); Carlo Olivieri and Francesco de Paulis (University of L'Aquila, Italy)

ABSTRACT
The increasing channel bandwidth requirements needed for next generation high-speed serial interfaces extends where notch stubs appear, due to tiny channel discontinuities previously negligible. The impact of such hanging stubs is exacerbated by nearby reference planes due to the parasitic capacitance of the loaded stub. Based on the example of a mated connector at the spring to pad interface, the analytical calculation of the fringing capacitance and of the corresponding downshift of the stub resonance is proposed. Practical examples are presented to demonstrate the need for predicting such frequency downshift.

TITLE	**Random Jitter Amplification Coefficient Calculation for NRZ PRBS Signal**
TIME	10:00-10:20 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Tao Wei, Yuhao Huang and Haiyue Yuan (Xidian University, China); Yuhuan Luo (Xi'an University of Posts and Telecommunications, Xi' an, Shaanxi, China); Jun Wang (Xidian University, China); Xiuqin Chu (Xidian University, China)

ABSTRACT
The effect of channel response on random jitter becomes more significant as the frequency of high-speed channels increases, further reducing the already diminished time margin in these channels. To accurately assess the impact of random jitter on the time margin, a novel methodology is proposed to calculate the random jitter amplification factor for Non-Return-to-Zero pseudo-random binary sequence (NRZ PRBS) signal and investigate the jitter amplification phenomenon. The simulated results based on 5th generation double data rate (DDR5) channels validate the effectiveness and accuracy of the proposed method.

TITLE	**Comprehensive Measurement-to-Simulation Methodology for Better Gigabit Interconnect Evaluation and Exploration**
TIME	10:40-11:00 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Tim Wang Lee, Mike Resso and JiWei Du (Keysight Technologies, USA)

ABSTRACT
At 100 Gb/s per lane, using measured data to explore design space is crucial, yet traditional workflows often keep measurement and simulation separate, slowing analysis and extending design iteration cycles. We present a unified, repeatable measurement-to-simulation methodology that closes this gap, turning raw VNA data into actionable design insight in hours instead of days. The process combines rigorous calibration, fixture removal, and de-embedding with high-fidelity channel modeling in simulation software. From a single multi-port S-parameter, engineers can extract material properties, identify impedance discontinuities, perform eye diagram analysis, and conduct behavioral modeling-based equalization studies for different modulation formats. Applied to gigabit interconnects, this approach accelerates analysis, reduces iteration cycles, and enhances confidence in meeting compliance, providing a standards-aligned path to improved signal integrity in next-generation designs.

TITLE	**Design Challenges and Optimization Strategies for High-Speed Connector Test Fixtures**
TIME	11:00-11:20 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Lei Deng (LinkE Technologies, China)

ABSTRACT
With the evolution of communication protocols such as PCIe and Ethernet toward higher speeds, test fixtures— the intermediate interconnect tools for verifying connector performance—face stringent challenges in core metrics: insertion loss (IL), crosstalk, and skew. This paper analyzes the technical bottlenecks of current test fixtures in high-frequency scenarios, relates them to recent protocol roadmaps (e.g., PCIe Gen6/Gen7 and 112G/224G Ethernet), and proposes practical future design optimizations.

TITLE	**High-Order Markov Modeling of DFE Error Propagation Under Residual ISI Using SBR-Derived Transitions**
TIME	11:20-11:40 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Yuhao Huang, Tao Wei and Haiyue Yuan (Xidian University, China); Yuhuan Luo (Xi'an University of Posts and Telecommunications, Xi' an, Shaanxi, China); Jun Wang (Xidian University, China); Xiuqin Chu (Xidian University, China)

ABSTRACT

As data rates continue to increase, signal-to-noise ratio (SNR) degradation caused by channel insertion loss and multiple noise sources exacerbates error propagation in decision feedback equalizer (DFE). Accurate bit error rate (BER) prediction under such conditions requires precise modeling of DFE error behavior in the presence of residual inter-symbol interference (ISI). This brief presents a high-order Markov modeling approach for DFE error propagation, in which state transition probabilities are analytically derived using the single-bit response (SBR) method. To enhance computational efficiency, the modeling process is accelerated by exploiting the DFE's decision characteristics and the sparsity of the transition matrix. Simulation results under various SNR scenarios demonstrate the accuracy of the proposed method.

TITLE	**Research on Physical Layer Signal Automated Testing Technology for Non-Standard Hardware Products**
TIME	11:40-12:00 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Chuangye Guo, Yuxu Huo and Chaoyu La (AVIC Xi'an Aeronautics Computing Technique Research Institute, China); Tingting Liu (Avic Xi'an Aeronautics Computing Technique Research Institute, China)

ABSTRACT

In view of the mismatch between the application expansion of non-standard hardware and traditional test methods in aerospace and electronic medical fields, this paper innovates a set of non-standard hardware automatic test system. Through the collaborative design of environmental configuration, test management and other modules, combined with the integration of programmable power supply, oscilloscope, vector network analyzer and other hardware. To achieve a technical breakthrough in the standardization of test process, intelligent data acquisition and automatic result analysis. In practical application, the test efficiency is improved by more than 40% compared with the traditional method, which effectively solves the problems of tedious configuration, inconsistent methods, and poor consistency of results in manual testing.

OVERVIEW OF SESSIONS II

SESSIONS	[SS2] Recent Advances in EMI/EMC Techniques
VENUE	HUALUXE Hall 1
TIME	13:20-15:20 November 6th
SESSION CHAIR	Si-Ping Gao, Nanjing University of Aeronautics and Astronautics Huapeng Zhao, University of Electronic Science and Technology of China
TECHNICAL TALKS	**Recent Progress of Fast Direct Partial Element Equivalent Circuit Method (Invited)** *Huapeng Zhao (University of Electronic Science and Technology of China, China)* **Suppressing Evanescent Wave Coupling Using Anisotropic Metasurface in Small Cavity Circuit (Invited)** *Da Yi, Wei Zhou and Jia-Qi He (Chongqing University, China); Hao Du and Wei Guo (ZTE, China); Huapeng Zhao (University of Electronic Science and Technology of China, China); Ming-Chun Tang (Chongqing University, China)* **Recent Advances in YIG-Based Frequency Selective Limiters** *Si-Ping Gao (Nanjing University of Aeronautics and Astronautics, China); Zequn Zeng (National University of Singapore, Singapore)* **A Reconfigurable Dual-Polarized Metasurface Capable of Switching Between Absorption and Transmission Modes** *Pei Zhang, Da Li and Er-Ping Li (Zhejiang University, China)* **Magnetic and Electric Shielding Effectiveness Measurement of System-in-Package** *Di Wang, Xing-Chang Wei and Ming-Jie Pang (Zhejiang University, China)* **S-Band Tunable Impedance Matching Network with Varactor Diodes** *Zhou Han, Xiong Chen and Bin Han (Xi'an Jiaotong University, China)*

TITLE	**Recent Progress of Fast Direct Partial Element Equivalent Circuit Method (Invited)**
TIME	13:20-13:40 November 6th
VENUE	HUALUXE Hall 1
AUTHOR	Huapeng Zhao, University of Electronic Science and Technology of China, China

ABSTRACT

Partial element equivalent circuit (PEEC) method is useful for interconnect modeling. For large scale interconnects, there are a large number of ports, whose PEEC modeling involves solution of matrix equation with multiple right-hand-sides (RHSs). In this case, iterative computation method leads to repetitive computation and wastes computation time. Direct method can avoid repetitive computation of iterative methods, but its computational complexity is high. Leveraging the low rank compression of rank-deficient matrix blocks, fast direct method can achieve fast matrix inversion and thus accelerate direct method. This talk presents recent progress of fast direct partial element equivalent circuit method. Numerical examples of large scale interconnects are shown to demonstrate the advantage of fast direct PEEC method.

BIOGRAPHY

Dr. Huapeng Zhao received the Ph.D. degree from Nanyang Technological University, Singapore, in June 2012. He was a Scientist with the A*STAR Institute of High Performance Computing, Singapore, from August 2011 to December 2015. Since December 2015, he has been with the University of Electronic Science and Technology of China, Chengdu, China, first as an Associate Professor, and promoted to a Full Professor in May 2021. He has authored or coauthored over 150 technical papers published in international journals or conferences. His current research interests include system-level electromagnetic analysis and design, and signal and data processing techniques in electromagnetics. Prof. Zhao received the IEEE APEMC Young Scientist Award and the URSI Young Scientist Award. He is currently a Young Editorial Board Member of Electromagnetic Science, and an Associate Editor of IEEE AWPL.

TITLE	**Suppressing Evanescent Wave Coupling Using Anisotropic Metasurface in Small Cavity Circuit (Invited)**
TIME	13:40-14:00 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Da Yi, Wei Zhou and Jia-Qi He (Chongqing University, China); Hao Du and Wei Guo (ZTE, China); Huapeng Zhao (University of Electronic Science and Technology of China, China); Ming-Chun Tang (Chongqing University, China)

ABSTRACT

In small cavity circuits with cross-section dimensions less than $0.5\lambda_0$, evanescent waves (EWs) dominate, but suppression of EWs has not been reported. This work proposes an anisotropic metasurface (AMS) design to cope with the problem. The AMS well enhance the EW attenuation below the cutoff of the cavity without introducing any negative parasitic effect. A third-order AMS design was proposed for the Sub-6G band circuits. It witnesses less than $0.1\lambda0$ transverse thickness and less than $0.15\lambda0$ profile. The 10-dB EW suppression bandwidth reaches 21.1%. The new design for the new EW suppression scenario can provide an effective solution for electromagnetic compatibility in small cavity circuits.

BIOGRAPHY

Da Yi (S'15 – M'19) received the B. S. degree and Ph. D. degree in electronic science and technology from Zhejiang University in 2014 and 2019, respectively. He currently works in Chongqing University, Chongqing, China as a professor.

Dr. Yi was the recipient of the awards in several international conferences, including Young Scientist award in APEMC 2022, Young Investigator Training Program (YITP) award in SPI 2017, Best Student Paper award in IWS 2016 and EMC COMPO 2019, Best Paper award in ISEMC 2019, and Best Presentation award in UCET 2021. His current research interest is the interference decoupling and noise suppression in antenna arrays and high-speed circuits.

TITLE	**Recent Advances in YIG-Based Frequency Selective Limiters**
TIME	14:00-14:20 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Si-Ping Gao (Nanjing University of Aeronautics and Astronautics, China); Zequn Zeng (National University of Singapore, Singapore)

ABSTRACT

This paper presents a non-exhaustive review of recent advances in Yttrium Iron Garnet (YIG)-based frequencyselective limiters (FSLs), emphasizing modeling methodologies and design strategies. The fundamental operating principles of YIG-based FSLs are first outlined, followed by a systematic categorization into reflective and absorptive types. For reflective-type FSLs, a novel design framework for the magnetostatic surface wave (MSSW) transmission line—the key enabling component—is introduced. This model allows for scalable and accurate prediction of S-parameters and facilitates optimization of impedance matching for wideband operation. Building on this foundation, a dual-matching approach is further proposed to enhance bandwidth while maintaining low insertion loss. Finally, the paper discusses the remaining challenges and emerging opportunities in integrating YIGbased FSLs into compact, wideband, and low-power RF frontend systems.

BIOGRAPHY

(Senior Member, IEEE) received the B.Eng., M.Eng. and D.Eng. degrees in electronic engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2007, 2009, and 2013, respectively.

From 2013 to 2017, he was a Scientist with the Department of Electronics and Photonics, Institute of High Performance Computing (IHPC), A*STAR, Singapore. From 2017 to 2022, he was a Research Fellow in the Department of Electrical and Computer Engineering, National University of Singapore (NUS). From 2022 to 2024, he was a Senior Engineer of AMD and concurrently an Adjunct Assistant Professor of NUS. He is currently a Full Professor of NUAA. He has authored more than 100 refereed papers and one book chapter. He holds several patents. His research interests include EMC/EMI, signal and power integrity for 2.5D/3D ICs, microwave ferrite devices and measurement.

Dr. Gao received the Young Professional Award from the IEEE EMC Society in 2021, the SPI 2017 Young Investigator Training Program Award, the URSI GASS 2017 Young Scientist Award, and the Outstanding Young Scientist Award at the 2018 Joint IEEE EMC & APEMC Symposium. He won the APEMC 2016 Best Symposium Paper Award and the IEEE MTT-S IMWS-AMP 2020 Best Paper Award. He served as the TPC Chair and TPC Co-chair of IEEE MTT-S IMWS-AMP 2025 and 2021, respectively, the Technical Paper Chair of APEMC 2022. He was a Guest Editor of IEEE TRANSACTIONS on MICROWAVE THEORY and TECHNIQUES (2025) and a Distinguished Reviewer of IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY (2023, 2024). He has been serving the IEEE EMC Singapore Chapter since 2016.

TITLE	**A Reconfigurable Dual-Polarized Metasurface Capable of Switching Between Absorption and Transmission Modes**
TIME	14:20-14:40 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Pei Zhang, Da Li and Er-Ping Li (Zhejiang University, China)

ABSTRACT
With the advent of the 6G communication era, electromagnetic interference among various communication devices has become increasingly severe. Multifunctional and reconfigurable metasurfaces offer a promising solution to meet the growing demand for electromagnetic protection. This paper presents a dual-polarized metasurface capable of switchable absorption–transmission modes, achieved by controlling the ON/OFF states of PIN diodes to realize functional conversion between absorption and transmission within a specific frequency band. The proposed metasurface consists of two planar layers embedded with PIN diodes. The first layer serves as a lossy layer that, in the OFF state of the diodes, enables efficient absorption and dissipation of electromagnetic waves, while in the ON state, it allows low-loss transmission. The second layer functions as a transmission layer that reflects electromagnetic waves when the diodes are ON and supports low-loss transmission when they are OFF. Through the synergistic effect of the two layers, the metasurface achieves an absorption rate exceeding 90% in the 3.4–11.7 GHz range, corresponding to a fractional bandwidth of 109.9%, and exhibits a transmission passband with insertion loss less than 3 dB within 8.6–9.4 GHz. This innovative design enables flexible electromagnetic wave manipulation in complex environments and provides a novel strategy for advanced electromagnetic protection applications.

TITLE	**Magnetic and Electric Shielding Effectiveness Measurement of System-in-Package**
TIME	14:40-15:00 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Di Wang, Xing-Chang Wei and Ming-Jie Pang (Zhejiang University, China)

ABSTRACT
Near field scanning system becomes a critical tool in electromagnetic compatibility (EMC) measurement, especially for measuring the shielding effectiveness (SE) of system-in-package (SiP). In this work, SE of an actual SiP is comprehensive assessed from magnetic, normal electric and tangential electric perspectives. All SE measurements exhibit a consistent trend, wherein they demonstrate superior performance when the penetration field is predominant, and conversely, exhibit diminished effectiveness when the leakage field becomes the dominant factor.

TITLE	**S-Band Tunable Impedance Matching Network with Varactor Diodes**
TIME	15:00-15:20 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Zhou Han, Xiong Chen and Bin Han (Xi'an Jiaotong University, China)

ABSTRACT
In this paper, we designed an impedance matching network works at a frequency of 2.4 GHz, which is the representative frequency of the S-band, and based on the three-stub impedance matching network. A varactor diode is added at the end of each stub serving as the tunable components. When there are some changes in the surrounding environment and causes mismatch, we can re-match it by adjusting the reverse bias applied to the varactor diode. The simulation results show that for a load of 120+j50Ω, when the bias voltage of the three varactor diodes is set to 2V, S11 at 2.4GHz can be reduced to less than -15dB. When the bias voltage is set to 2.3, 1.3, and 1.8Vrespectively, S11 can be reduced to less than -40dB at 2.4GHz. When the real part changes between 40~200Ω, or the imaginary part changes between -150~150Ω, S11 at 2.4GHz can also be reduced to below -40dB by giving an appropriate voltage to achieve impedance matching.

OVERVIEW OF SESSIONS III

SESSIONS	[SS3] Advance in Electromagnetism Simulation and Analysis Method
VENUE	HUALUXE Hall 3
TIME	8:40-12:00 November 6th
SESSION CHAIR	Xiong Chen, Xi'an Jiaotong University, China Xiuqin Chu, Xidian University, China
TECHNICAL TALKS	**Exploring Advanced Packaging in 2.5D/3D IC EDA: A Unified Platform for Backend Physical Design Simulation and Verification (Invited)** *Yi Zhao, Zhuhai Silicon Chip Technology Ltd., China* **Fast EM Algorithms for Interconnects in 2.5D/3D Integrated Circuits (Invited)** *Shunchuan Yang, Beihang University, China* **Physics-Constrained Differential Evolution for Continuous Decoupling Capacitor Placement and Orientation Optimization** *Li Jiang, Ling Zhang, Junjie Ren, Keyi Ding and Er-Ping Li (Zhejiang University, China)* **Dielectric Reconfigurable S-band Planar Phase Shifter** *Yichen Liu, Xiong Chen and Han Yu (Xi'an Jiaotong University, China); Jun Fan (Missouri University of Science and Technology, USA); David Pommerenke (TU Graz, Austria)* **Analysis of the Influence of Three - Proof Coating on the High - Speed Signal Transmission Performance of Embedded Computers** *Zichun Zhang (Xi'an Aeronautics Computing Technique Research Institute, China); Tingting Liu (Avic Xi'an Aeronautics Computing Technique Research Institute, China); Yuxu Huo (AVIC Xi'an Aeronautics Computing Technique Research Institute, China)* **An Equation Based Solver for High-Speed Differential Pairs Affected by Fiber Weave Effect** *Kai Li (Cisco Systems, Inc., China); Felen Fu (Cisco Systems, Inc, China); Yan Li (Cisco Systems, Inc., China); Xiao-Ding Cai and Bidyut Sen (Cisco Systems, Inc, USA)* **An Integrated Simulation Software for Component EMC Design and Analysis** *Jianhao Ge, Zhaowen Yan, Tengfei Gao, zeyu Han, Jingqi Lu and Yifan Zhen (Beihang University, China)* **Liquid Gated Network-Based Signal Integrity Analysis for High-Speed Links** *Yuxiang Tian and Jiarui Qiu (Zhejiang University, China); Yiqin Xiang (Zhejiang University, China & University of Illinois Urbana-Champaign, USA); Er-Ping Li and Hanzhi Ma (Zhejiang University, China)* **Addressing the Radio Frequency Interference Problem Through Characteristic Mode Analysis** *Xu Wang (Zhejiang University, China); Xiaoping Li (Swust University, China); Xinglin Sun (Zhejiang University, China); Tingting Liu and Shiming Qin (Xi'an Aeronautical Computing Technology Research Institute, China)*

TITLE	**Exploring Advanced Packaging in 2.5D/3D IC EDA: A Unified Platform for Backend Physical Design Simulation and Verification (Invited)**
TIME	08:40-09:00 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Yi Zhao, Zhuhai Silicon Chip Technology Ltd., China

ABSTRACT

The use of advanced packaging technologies, such as Chiplets and 2.5D/3D IC stacking, is driving a significant shift in the semiconductor industry. These innovations tackle key challenges in chip design and manufacturing, including memory, power, and space limitations, creating new opportunities for the industry's future. However, these advancements also bring new challenges. From both physical design and simulation verification perspectives, the next generation of stacked chip EDA tools places unprecedented demands on the design process. For example, dealing with new structures like TSVs represents a major step forward compared to traditional tools. At the same time, the integration of multi-die and TSVs exponentially increases design complexity and computational requirements. Additionally, the ultra-high density heterogeneous integration brought by Chiplet advanced packaging has significantly increased the difficulty of multi-physics simulations such as thermoelectric, magnetic, and electric fields.

This presentation will conduct an in-depth analysis of these challenges, explore potential solutions, and elaborate on SiChip 's self-developed 3Sheng Integration stacked chip EDA platform. The platform features a dual-system collaborative optimization framework, anchored by "Chiplet-Interposer-Packaging Co-design" and "Performance-Cost-Testability Co-optimization", and has established a full-flow toolchain encompassing five core centers: 3Sheng Zenith (Architecture Design) – 3Sheng Ranger (Physical Implementation) – 3Sheng Ocean (Multi-die DFT) – 3Sheng Volcano (Co-Simulation) – 3Sheng Stratify (Multi-die Physical Verification)(LVS and DRC).Furthermore, it will share technical advancements in key domains including multi-chip integrated system modeling, Chiplet physical design, multi-physics simulation , Chiplet verification, and test fault tolerance tailored for advanced packaging. Through these insights, we aim to enable the audience to gain a more comprehensive understanding of the application and development of next-generation 2.5D/3D IC EDA tools.

BIOGRAPHY

Holding a Ph.D. from the University of Southampton, UK, under the supervision of Royal Society Fellow Professor Bashir Hashimi, he embarked on 2.5D/3D stacked IC design research in 2008 as part of one of the world's earliest pioneering research teams exploring advanced chip architecture methodologies, having collaborated with IMEC for 3D-IC technology validation. With 15 years of dedicated R&D in 3D integrated circuit design, he has published several excellent papers and awarded the VLSI-SOC Best Paper.

Currently serving as Founder and Chief Scientist at Zhuhai Silicon Chip Technology Ltd., he has been a majority of leading national research initiatives. He directs the team in developing self-proprietary 2.5D/3D Stacked IC EDA tools, enabling critical advancements in the semiconductor industry through backend full-flow EDA tools and solutions.

TITLE	**Fast EM Algorithms for Interconnects in 2.5D/3D Integrated Circuits (Invited)**
TIME	09:00-09:20 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Shunchuan Yang, Beihang University, China

ABSTRACT

The current trend in integrated circuits is shifting from two-dimensional (2D) to three-dimensional (3D) integration, leading to a significant increase in the density of interconnects. Rapid and accurate extraction of circuit parameters serves as a crucial foundation for signal integrity and power integrity design. This presentation mainly introduces our group's work on the electric field integral equation (EFIE) method combined with field–circuit co-analysis, as well as its applications in the fast extraction of parasitic parameters for 2.5D/3D integrated circuits.

BIOGRAPHY

Dr. Shunchuan Yang received the B.S. degree from Sichuan University, Chengdu, China, in 2009, the M.S. degree from Zhejiang University, Hangzhou, China, in 2012, and the Ph.D. degree from Dalhousie University, Halifax, NS, Canada, in 2015. He continued his research as a Post-Doctoral Fellow with the University of Toronto, Toronto, ON, Canada, and joined Beihang University, Beijing, China, in 2017, where he is currently an Associate Professor. His research interests are development of advanced numerical methods and their applications in fast parameter extraction for 2.5D/3D integrated circuits and simulations of electrically large-scale/multiscale structures in electromagnetics.

Dr. Yang was a recipient of the Young Scientist Award of the 2022 Asia-Pacific International Symposium on Electromagnetic Compatibility and Signal Integrity and the 2019 Applied Computational Electromagnetics Society China. 13 students' papers under his supervision were selected as Finalists for the Student Paper Competition and won the Honorable Mention Award in the 2021/2022/2023 International Applied Computational Electromagnetics Society (ACES) Symposium and the 2021/2022/2023 IEEE International Symposium on Antennas and Propagation.

TITLE	**Physics-Constrained Differential Evolution for Continuous Decoupling Capacitor Placement and Orientation Optimization**
TIME	09:20-09:40 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Li Jiang, Ling Zhang, Junjie Ren, Keyi Ding and Er-Ping Li (Zhejiang University, China)

ABSTRACT

The layout of decoupling capacitors (decaps) is essential for the performance of power distribution networks (PDNs). This article proposes a novel decap layout optimization method for PDN design considering the decap location, orientation, package size, and type selection. A differential evolution (DE) algorithm is employed to determine the layout configuration for a given number of decaps. Decaps are iteratively placed within the PDN area, and the corresponding layout is optimized using the DE algorithm until the target impedance is satisfied. The proposed method achieves an efficient and physically consistent layout configuration, providing a compact design with an optimized number of decaps while maintaining the desired PDN performance.

TITLE	**Dielectric Reconfigurable S-band Planar Phase Shifter**
TIME	09:40-10:00 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Yichen Liu, Xiong Chen and Han Yu (Xi'an Jiaotong University, China); Jun Fan (Missouri University of Science and Technology, USA); David Pommerenke (TU Graz, Austria)

ABSTRACT
This paper proposes a planar dielectric-based tuning phase shifter. Phase tuning is achieved through the mechanical displacement of the dielectric material perpendicular to the direction of signal propagation. To maintain low reflection during the tuning process, a multi-stage cascaded structure is introduced to create design tolerance, and the ADAM gradient descent algorithm is employed for structural optimization. Simulation results demonstrate a phase shift range of 186 ° @ 2.4GHz with a return loss better than 29 dB.

TITLE	**Analysis of the Influence of Three - Proof Coating on the High - Speed Signal Transmission Performance of Embedded Computers**
TIME	10:00-10:20 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Zichun Zhang (Xi'an Aeronautics Computing Technique Research Institute, China); Tingting Liu (Avic Xi'an Aeronautics Computing Technique Research Institute, China); Yuxu Huo (AVIC Xi'an Aeronautics Computing Technique Research Institute, China)

ABSTRACT
With the rapid development of modern military technology, military embedded computers are increasingly widely used in complex battlefield environments. To ensure its stable operation under harsh conditions, the three-proof (waterproof, dustproof and anti-corrosion) design becomes crucial. However, while the three-proof coating enhance the environmental adaptability of the equipment, it may also impacts the performance of high-speed signal transmission. This paper, through theoretical analysis and simulation research, deeply explores the performance differences of highspeed signal transmission before and after the three-proof coating of military embedded computers, aiming to optimize the design of military embedded computers. It provides theoretical basis and technical support for achieving a balance between three-proof performance and high-speed signal transmission performance.

TITLE	**An Equation Based Solver for High-Speed Differential Pairs Affected by Fiber Weave Effect**
TIME	10:40-11:00 November 6th
VENUE	HUALUXE Hall 3
AUTHORSv	Kai Li (Cisco Systems, Inc., China); Felen Fu (Cisco Systems, Inc, China); Yan Li (Cisco Systems, Inc., China); Xiao-Ding Cai and Bidyut Sen (Cisco Systems, Inc, USA)

ABSTRACT
In this paper, the close-formula method is proposed and improved for the analysis of print circuit board (PCB) cross sections with inhomogeneous dielectric constant (Dk). The mathematical modeling method is used to obtain the accurate fiber-weave structure in PCB. The Dk values required for cross-section analysis are derived from the projection method. Finally, an equation-based solver for high-speed differential pairs affected by fiber-weave effect (FWE) is proposed. The accuracy and efficiency of proposed solver are verified by comparing the simulation results between the equation-based solver and the commercial 3-dimensional (3D) tool. The proposed solver shows comparable accuracy and is approximately 180 times more efficient than the commercial 3D tool.

TITLE	**An Integrated Simulation Software for Component EMC Design and Analysis**
TIME	11:00-11:20 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Jianhao Ge, Zhaowen Yan, Tengfei Gao, zeyu Han, Jingqi Lu and Yifan Zhen (Beihang University, China)

ABSTRACT
In response to the increasingly severe challenges of modern electronic products, this paper introduces an advanced simulation design software for electromagnetic compatibility (EMC) and protection of components. The software integrates core functional modules such as conducted emission (CE) model generation, conducted immunity (CI) model generation, radiated emission (RE) model generation, and electromagnetic vulnerability (EMV) model generation. It also features a built-in model library and circuit simulation module, providing electronic designers with a comprehensive simulation and analysis platform. Using this tool, engineers can accurately predict and evaluate the EMC performance of products in the early design stages, identify potential electromagnetic interference issues, and effectively design protection solutions. The software significantly improves the first-pass success rate of products, shortens development cycles, and reduces the costs associated with rectifying EMC issues, offering substantial value for the development of highperformance and high-reliability electronic devices.

TITLE	**Liquid Gated Network-Based Signal Integrity Analysis for High-Speed Links**
TIME	11:20-11:40 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Yuxiang Tian and Jiarui Qiu (Zhejiang University, China); Yiqin Xiang (Zhejiang University, China & University of Illinois Urbana-Champaign, USA); Er-Ping Li and Hanzhi Ma (Zhejiang University, China)

ABSTRACT
With the continuous increase in microsystem integration density and data transmission rates, signal integrity analysis of high-speed links has become increasingly important. Traditional SPICE simulation is accurate but extremely timeconsuming. Neural network–based surrogate models offer fast prediction of signal integrity, yet conventional recurrent methods struggle to capture subtle signal variations. This paper proposes the Liquid Gated Network (LGN) method and validates its performance through a practical high-speed link.

TITLE	**Addressing the Radio Frequency Interference Problem Through Characteristic Mode Analysis**
TIME	11:40-12:00 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Xu Wang (Zhejiang University, China); Xiaoping Li (Swust University, China); Xinglin Sun (Zhejiang University, China); Tingting Liu and Shiming Qin (Xi'an Aeronautical Computing Technology Research Institute, China)

ABSTRACT
Noise generated by digital circuits leads to radio frequency interference problems. The physics-based dipole moment model and the transfer function method are commonly used for interference analysis and mitigation. Herein, the characteristic mode is used to derive the short-circuit noise current on the antenna port in the transfer function calculation. Through use of the simplified modal weighting coefficient formulation for dipole moment excitation, the interaction between the noise source and the characteristic modes can be quantified according to the modal analysis results. Decomposing the induced short-circuit current on the antenna port into the contributions of different modes enables identification of the critical mode in the interference. Mitigation strategies are then proposed on the basis of the modal near-field information.

OVERVIEW OF SESSIONS IV

SESSIONS	[SS4] Power Integrity Design Techniques
VENUE	HUALUXE Hall 1
TIME	15:40-17:40 November 6th
SESSION CHAIR	Jun Wang, Xidian University, China Xinglin Sun, Zhejiang University, China
TECHNICAL TALKS	**A Hierarchical Optimization and Learning Framework for Broadband MLCC Equivalent-Circuit Modeling** *Yongjie Chen (Zhejiang University, China); Zhou Jin (Zhejaing University, China); Cheng Zhuo (Zhejiang Univ, China)* **Calculation Method for Statistical Distribution of Power Supply Noise in Chip-Package-PCB Co-Design** *Yuhuan Luo (Xi'an University of Posts and Telecommunications, Xi' an, Shaanxi, China); Haiyue Yuan, Yajun Lv and Xiuqin Chu (Xidian University, China); Jun Wang (Xidian University, China)* **Multi-Objective Decap Optimization Based on Non-Dominated Sorting Genetic Algorithm** *Keyi Ding, Ling Zhang, Li Jiang, Junjie Ren and Er-Ping Li (Zhejiang University, China)* **Overestimation of Inductance in PDN Modeling: A Study on MLCC Models** *Cailiang Fu (Southwest University of Science and Technology, China); Anfeng Huang and Yin Sun (DeTooLIC Technology Co., China); Guozheng Zhang, Jie Li and Junfeng Luo (Southwest University of Science and Technology, China)* **Attention-Guided Reinforcement-Genetic Optimizer: Fast PDN Impedance Prediction and Decoupling Capacitor Design for Power Integrity** *Qiyu Jiang and Shufang Li (Beijing University of Posts and Telecommunications, China)* **Simulation and Test of 112Gbps SerDes Power Noise** *Lingyun Liu, Jianguo Zhang, Bin Yu, Shuangman Xie and Erling Pan (SANECHIPS Technology CO. LTD, China); Zhijun Long (Sanechips Technology Co. Ltd, China)*

TITLE	**A Hierarchical Optimization and Learning Framework for Broadband MLCC Equivalent-Circuit Modeling**
TIME	15:40-16:00 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Yongjie Chen (Zhejiang University, China); Zhou Jin (Zhejaing University, China); Cheng Zhuo (Zhejiang University, China)

ABSTRACT

This paper introduces a broadband, operating-condition-aware modeling framework for multilayer ceramic capacitors (MLCCs). The framework integrates a scalable equivalent-circuit topology with hierarchical optimization and Gaussian Process Regression (GPR). The proposed topology enhances the conventional four-element model by incorporating RC/RL ladder subnetworks to capture non-monotonic ESR behavior and parallel RLC branches to represent multiple anti-resonance peaks. A hierarchical optimization strategy is employed to decompose the high-dimensional parameter extraction process into manageable subproblems, thereby improving both convergence and accuracy. To facilitate predictions under arbitrary DC bias and temperature conditions without requiring exhaustive measurements, GPR is utilized to learn a nonlinear mapping between operating conditions and circuit parameters. Experimental validation conducted on hundreds of MLCCs demonstrates that the proposed model reduces impedance magnitude mean relative errors (MREs) by an order of magnitude compared to the four-element model. Furthermore, GPR achieves prediction errors below 1.3%, underscoring the framework's accuracy, efficiency, and applicability for power and signal integrity design.

TITLE	**Calculation Method for Statistical Distribution of Power Supply Noise in Chip-Package-PCB Co-Design**
TIME	16:00-16:20 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Yuhuan Luo (Xi'an University of Posts and Telecommunications, Xi' an, Shaanxi, China); Haiyue Yuan, Yajun Lv and Xiuqin Chu (Xidian University, China); Jun Wang (Xidian University, China)

ABSTRACT

This paper innovatively proposes a detailed estimation scheme for determining the statistical distribution of power supply voltage noise based on multi-pulse responses. The current excitation for a chip load is first divided into a superposition of multi-pulse current by the piecewise linear method and encoded. Then, the statistical voltage noise distribution of the power distribution network is calculated by using the responses of multi-pulse currents. The proposed method is compared with the brute-force simulation method and shows consistent advantages in calculating statistical voltage noise. By calculating the statistical probability of voltage noise, engineers can predict when a system fault might occur, aiding engineers in preventive maintenance or preemptive system restarts to prevent actual faults.

TITLE	**Multi-Objective Decap Optimization Based on Non-Dominated Sorting Genetic Algorithm**
TIME	16:20-16:40 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Keyi Ding, Ling Zhang, Li Jiang, Junjie Ren and Er-Ping Li (Zhejiang University, China)

ABSTRACT
Optimizing power distribution networks (PDNs) is a key research target in power integrity (PI) design, and the optimization of decoupling capacitors (decaps) is a critical approach to designing the PDN and meeting its design requirements. This paper proposes a multi-objective decap optimization method based on a non-dominated sorting genetic algorithm II (NSGA-II). The method employs a port priority algorithm to find better initial solutions, and it can obtain better Pareto frontier solutions than the traditional weighted sum objective function within the same time frame.

TITLE	**Overestimation of Inductance in PDN Modeling: A Study on MLCC Models**
TIME	16:40-17:00 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Cailiang Fu (Southwest University of Science and Technology, China); Anfeng Huang and Yin Sun (DeTooLIC Technology Co., China); Guozheng Zhang, Jie Li and Junfeng Luo (Southwest University of Science and Technology, China)

ABSTRACT
With the emergence of artificial intelligence (AI) applications, power consumption has become increasingly critical in state-of-the-art server designs. To accommodate the voltage droop and overshoot generated by the varying current of GPUs, the impedance of the power delivery network (PDN) must be well controlled within the milliohm range. Consequently, the impedance of decoupling capacitors, such as multi-layer ceramic capacitors (MLCCs), needs to be accurately evaluated during the design stage. It is important to emphasize that the PDN impedance associated with MLCCs is closely related to capacitor installation methods and PCB design. This dependency prevents supplier-provided capacitor models from being directly integrated with existing simulation tools. In this paper, we compare simulations and measurements of the PDN under different PCB designs with varied capacitor placements. Our findings indicate that the existing PDN design flow tends to overestimate the equivalent inductance introduced by capacitors; in the cases we validated, this overestimation can reach up to 40%.

TITLE	**Attention-Guided Reinforcement-Genetic Optimizer: Fast PDN Impedance Prediction and Decoupling Capacitor Design for Power Integrity**
TIME	17:00-17:20 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Qiyu Jiang and Shufang Li (Beijing University of Posts and Telecommunications, China)

ABSTRACT

Automating decoupling capacitor design for power distribution networks (PDNs) is fundamentally limited by a search evaluation bottleneck: fast optimizers must repeatedly call slow, high-fidelity electromagnetic simulations. We address this bottleneck by decoupling physics prediction from optimization. An offline phase trains a high-fidelity, wideband surrogate (the AI Physics Engine) on boundary-element solver data; an online phase lets the ARGO (Attention-guided Reinforcement–Genetic Optimizer) agent use this engine for near-instant impedance evaluation. ARGO employs a parallel GA–DQN architecture with attention-based knowledge fusion. The decoupled paradigm reduces per-evaluation latency to 1.2ms (a speedup of 8.3e3 over BEM) and, on a benchmark PCB with 29 candidate decap sites, meets the target with 7 capacitors in 1.1min; across five unseen boards it outperforms pure GA, pure DQN, and a sequential GA→DQN hybrid, enabling a reusable drop-in replacement for the EM solver inside EDA optimization loops.

TITLE	**Simulation and Test of 112Gbps SerDes Power Noise**
TIME	17:20-17:40 November 6th
VENUE	HUALUXE Hall 1
AUTHORS	Lingyun Liu, Jianguo Zhang, Bin Yu, Shuangman Xie and Erling Pan (SANECHIPS Technology CO. LTD, China); Zhijun Long (Sanechips Technology Co. Ltd, China)

ABSTRACT

Compared with traditional parallel transmission technology, serial transmission technology can fully utilize the channel capacity of communication channels, improve communication speed, and significantly reduce communication costs. SerDes (Serializer/Deserializer) is an integrated circuit technology that converts parallel data into high-speed serial data (transmitter) and restores serial data into parallel data (receiver), used to solve timing, noise, and distance issues in high-speed data transmission. Noise cannot be completely eliminated, and interference sources include circuit design, layout and wiring, as well as electron and hole characteristics. As the signal frequency increases, the impact of noise becomes greater, and the need to minimize noise becomes stronger. Based on practical project experience, this article introduces the noise simulation and testing of SerDes interface from the perspective of power supply noise simulation and testing principles. The noise simulation error of digital power supply and analog power supply is less than 3mV, achieving highprecision noise simulation consistency alignment.

OVERVIEW OF SESSIONS V

SESSIONS	[SS5] AI/ML based EMC/SI/PI Design
VENUE	HUALUXE Hall 3
TIME	13:20-15:20 November 6th
SESSION CHAIR	Dawei Wang, Hangzhou Dianzi University, China Xiaohe Chen, China University of Petroleum, China
TECHNICAL TALKS	**Application of Optimization Algorithms in Channel Signal Integrity Design** *Qihang Shang, Wenzhi Wang, Yade Fang and Yanwu Wang (DeTooLIC Ltd. Technology, China); Yi Chen (ZTE Corporation, China)* **High-Speed Link Surrogate Modeling Based on Multimodal Machine Learning** *XiaoYang Wu (Hang Zhou Dian Zi University, China); Wen-Sheng Zhao and Da-Wei Wang (Hangzhou Dianzi University, China)* **An Efficient Thermal-Aware Placement Method for Chiplet-Oriented Integrated Microsystems** *Peng Zhang, Da-Wei Wang and Wen-Sheng Zhao (Hangzhou Dianzi University, China)* **Machine Learning-Assisted S-Parameter Frequency-Domain Extrapolation Method** *Fei Zhou, Wen-Sheng Zhao and Da-Wei Wang (Hangzhou Dianzi University, China)* **DNN-Based Prediction of Frequency-Dependent RLGC Parameters for Transmission Lines** *Jiaqi He (Xidian University, China); Rongyao Tang (Fiberhome Telecommunication Technologies Co., Ltd, China); Kuan Zhang (DeTooLIC Technology Co., Ltd, China); Mengyao Ai (Fiberhome Telecommunication Technologies Co., Ltd, China); Xiaohe Chen (China University of Petroleum, China); Xiuqin Chu (Xidian University, China); Jun Fan and Bo Pu (DeTooLIC Technology Co., Ltd, China)* **PCB Stack-Up Recognition Using LLMs** *Jie Li (Southwest University of Science and Technology, China); Shiming Qin and Tingting Liu (Xi'an Aeronautical Computing Technology Research Institute, China); Yuyu Zhu, Haoran Li and Cailiang Fu (Southwest University of Science and Technology, China)*

TITLE	**Application of Optimization Algorithms in Channel Signal Integrity Design**
TIME	13:20-13:40 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Qihang Shang, Wenzhi Wang, Yade Fang and Yanwu Wang (DeTooLIC Ltd. Technology, China); Yi Chen (ZTE Corporation, China)

ABSTRACT
The artificial intelligence (AI) revolution is driving an explosive increase in data transmission and computational bandwidth demands, intensifying challenges in signal integrity (SI) design. Traditional approaches, such as Design of Experiments (DoE), are widely used to evaluate channel performance and identify optimal parameter configurations. However, the second-order Response Surface Model (RSM) used in the standard DoE workflow may lack accuracy when dealing with numerous parameters across wide tuning ranges. To overcome this limitation, this paper investigates the application of two algorithms for SI system optimization: Sequential DoE (SDoE) and Bayesian optimization (BO). We compare their performance in optimizing a high-speed channel. BO demonstrates superior computational efficiency and the crucial flexibility to handle both discrete and continuous variables, making it ideal for complex, real-world designs. On the other hand, SDoE generates an explicit and interpretable system model, offering deeper physical insights. The choice of method therefore depends on the primary engineering goal: maximum efficiency and design flexibility versus in-depth system understanding.

TITLE	**High-Speed Link Surrogate Modeling Based on Multimodal Machine Learning**
TIME	13:40-14:00 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	XiaoYang Wu (Hang Zhou Dian Zi University, China); Wen-Sheng Zhao and Da-Wei Wang (Hangzhou Dianzi University, China)

ABSTRACT
With the advancement of very-large-scale integration, high-speed interconnects face growing signal integrity (SI) challenges. Traditional simulation methods are computationally expensive and inefficient. This paper proposes a multimodal machine learning-based surrogate model for transient analysis of high-speed links. Long short-term memory, graph convolutional, and deep neural networks extract features from the transmitter, channel, and receiver, respectively. A cross-channel attention mechanism adaptively fuses multimodal features to improve prediction accuracy. The approach significantly reduces simulation cost while maintaining high modeling accuracy, demonstrating strong potential for efficient high-speed link design.

TITLE	**An Efficient Thermal-Aware Placement Method for Chiplet-Oriented Integrated Microsystems**
TIME	14:00-14:20 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Peng Zhang, Da-Wei Wang and Wen-Sheng Zhao (Hangzhou Dianzi University, China)

ABSTRACT
To enhance the efficiency and effectiveness of chiplet-oriented thermal-aware placement, a thermal predictor based on artificial neural networks is constructed. To achieve sufficient training of surrogate model, the collected dataset is expanded through a proposed data augmentation method based on coordinate transformation. A hybrid improved adaptive genetic algorithm-simulated annealing algorithm is employed to enhance the bias towards global/local optimization, thereby propelling thermal-aware design. The enhanced thermal-aware design approach is compared with other methods from multiple perspectives. The 8.7% and 5.4% enhancement in convergence and 4.2x speedup demonstrates improvements in both design effectiveness and efficiency.

TITLE	**Machine Learning-Assisted S-Parameter Frequency-Domain Extrapolation Method**
TIME	14:20-14:40 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Fei Zhou, Wen-Sheng Zhao and Da-Wei Wang (Hangzhou Dianzi University, China)

ABSTRACT
To tackle the high cost and bandwidth limitations in high-frequency S-parameter measurement, this paper proposes a machine learning-based frequency-domain extrapolation method. A multi-head convolutional neural network-long short-term memory network transfer learning model establishes a nonlinear mapping from low- to highfrequency S-parameters, incorporating geometric parameters as auxiliary inputs. The model supports parallel extrapolation of multiple S-parameters and employs transfer learning from circuit to EM simulations to enhance generalization under small-sample conditions. Validated on representative interconnect structures, the method exhibits good extrapolation performance across a wide frequency range.

TITLE	**DNN-Based Prediction of Frequency-Dependent RLGC Parameters for Transmission Lines**
TIME	14:40-15:00 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Jiaqi He (Xidian University, China); Rongyao Tang (Fiberhome Telecommunication Technologies Co., Ltd, China); Kuan Zhang (DeTooLIC Technology Co., Ltd, China); Mengyao Ai (Fiberhome Telecommunication Technologies Co., Ltd, China); Xiaohe Chen (China University of Petroleum, China); Xiuqin Chu (Xidian University, China); Jun Fan and Bo Pu (DeTooLIC Technology Co., Ltd, China)

ABSTRACT
In high-speed interconnect design in printed circuit board (PCB) and package, parameter sweep in simulation is essential to keep critical transmission line metrics within specifications, yet traditional methods for extracting perunit- length resistance, inductance, conductance, and capacitance (P.U.L. RLGC) incur significant computational burden in multi-dimensional simulation, while machine learning methods have not widely considered for frequency characteristics. To solve this issue, this study proposes a frequency dependent RLGC model to predict wideband P.U.L. RLGC parameters with neural networks. Four types of transmission lines are applied to the model and demonstrate both high prediction accuracy (R-Square above 98.80%), and substantial computational efficiency (20+ times faster).

TITLE	**PCB Stack-Up Recognition Using LLMs**
TIME	15:00-15:20 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Jie Li (Southwest University of Science and Technology, China); Shiming Qin and Tingting Liu (Xi'an Aeronautical Computing Technology Research Institute, China); Yuyu Zhu, Haoran Li and Cailiang Fu (Southwest University of Science and Technology, China)

ABSTRACT
With the increasing integration of electronic products, printed circuit board (PCB) are evolving toward higher speeds and more layered structures. However, the diversity of stack-up rules has led to significant challenges in the interoperability of design simulation and manufacturing processes across different vendors and users. To address this issue, this paper proposes an intelligent stack-up recognition method based on large language models (LLMs), which automatically converts PCB stack-up information into a standardized format defined by users or manufacturers. Experimental results demonstrate that online LLMs with over 500 billion parameters achieve a high recognition accuracy, exceeding 92%. In scenarios demanding data confidentiality or facing computational constraints, locally deployed lightweight models are a preferable alternative. However, models with no more than 8 billion parameters exhibit a significantly lower accuracy of below 37%, which is insufficient for practical purposes. Therefore, further investigation is essential to improve the viability of local lightweight models for this application.

OVERVIEW OF SESSIONS VI

SESSIONS	[SS6] Antenna Design Techniques
VENUE	HUALUXE Hall 3
TIME	15:40-17:40 November 6th
SESSION CHAIR	Guangxiao Luo, North China Electric Power University (Baoding) Syed Muzahir Abbas, Macquarie University, Australia
TECHNICAL TALKS	**An Efficient 2D/3D Mesh-Coupled Electro-Thermal Co-Simulation Method for Large-Scale Integrated Millimeter-Wave Phased Arrays** *Xinhong Xie (Donghai Laboratory, China); Zixian Ma and Haotian Chen (Zhejiang University, China); Hangkai Zhang and Gaofeng Cai (DeTooLIC Ltd., China); Yin Sun (DeTooLIC Technology Co., China); Bo Pu (DeTooLIC Ltd., China); Nayu Li, Chunyi Song and Zhiwei Xu (Zhejiang University, China)* **Computational Modeling of a Microstrip Antenna and Measurements with a Nano VNA** *Kenedy Marconi Geraldo Santos and Lucas dos Santos Ribeiro (IFBA, Brazil); Marcelo B Perotoni (UFABC, Brazil); José Amado (FEDERAL INSTITUTE OF BAHIA & IFBA, Brazil); Crescencio L. R. Neto (IFBA, Brazil); Tagleorge Marques Silveira (Instituto de Telecomunicações - IT & Universidade de Aveiro, Portugal)* **CPW Antenna for Satellite Earth Mapping and Radiolocation Systems** *Marcelo B Perotoni (UFABC, Brazil); Tagleorge Marques Silveira (Instituto de Telecomunicações - IT & Universidade de Aveiro, Portugal); Kenedy Marconi Geraldo Santos (IFBA, Brazil); José Amado (FEDERAL INSTITUTE OF BAHIA & IFBA, Brazil); Crescencio L. R. Neto and Lucas dos Santos Ribeiro (IFBA, Brazil)* **Dual Wideband Metasurface Based Linear to Circular Polarizer for Transmission Mode** *Fatima Ghulam (Zhejiang Normal University, China); Hajra Khan (Comsats University Islamabad Abbottabad Campus, Pakistan); Farman Ali Mangi (Shah Abdul Latif University Khairpur, Pakistan); Syed Muzahir Abbas (Macquarie University, Australia)* **Spiral Blade-Inspired Polarization-Insensitive X-Band FSS for EMI Shielding Applications** Saad Hassan Kiani (Universiti Teknikal malaysia, Melaka, Malaysia); Altaf Ahmed (Universiti Teknikal Malaysia Melaka (UTeM), Malaysia); Muhammad Ikram (American University of Kuwait, Kuwait); Umair Rafique (University of Oulu, Finland); Imran Mohd Ibrahim (Universiti Teknikal Malaysia Melaka, Malaysia); Syed Muzahir Abbas (Macquarie University, Australia) **Calibration of Simple Transient Electric Field Probe and Circuit-Based Waveform Reconstruction** *Guangxiao Luo, Yizhe Zhang and Yuhang He (North China Electric Power University (Baoding), China)*

TITLE	**An Efficient 2D/3D Mesh-Coupled Electro-Thermal Co-Simulation Method for Large-Scale Integrated Millimeter-Wave Phased Arrays**
TIME	15:40-16:00 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Xinhong Xie (Donghai Laboratory, China); Zixian Ma and Haotian Chen (Zhejiang University, China); Hangkai Zhang and Gaofeng Cai (DeTooLIC Ltd., China); Yin Sun (DeTooLIC Technology Co., China); Bo Pu (DeTooLIC Ltd., China); Nayu Li, Chunyi Song and Zhiwei Xu (Zhejiang University, China)

ABSTRACT

This paper proposes an efficient 2D/3D meshcoupled electro-thermal co-simulation method tailored for high-density printed circuit boards (PCBs) in large-scale, highly integrated millimeter-wave phased arrays for low Earth orbit (LEO) satellite communication systems. By leveraging 2D finite-element discretization for direct current (DC) analysis and a coarse block-based 3D finite-element model for thermal simulation, coupled via a projection-based data transfer scheme, the framework significantly reduces computational cost while maintaining high accuracy. Validation against a commercial solver (Cadence PowerDC) shows excellent agreement in current, voltage, and temperature results—yet the proposed method achieves these results in only 33% of the CPU time and 90% of the memory consumption required by PowerDC. The proposed method thus achieves a favorable trade-off between accuracy and speed. It is particularly well-suited for large-scale, highdensity PCBs where full 3D multiphysics simulations are computationally prohibitive.

TITLE	**Computational Modeling of a Microstrip Antenna and Measurements with a Nano VNA**
TIME	16:00-16:20 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Kenedy Marconi Geraldo Santos and Lucas dos Santos Ribeiro (IFBA, Brazil); Marcelo B Perotoni (UFABC, Brazil); José Amado (FEDERAL INSTITUTE OF BAHIA & IFBA, Brazil); Crescencio L. R. Neto (IFBA, Brazil); Tagleorge Marques Silveira (Instituto de Telecomunicações - IT & Universidade de Aveiro, Portugal)

ABSTRACT

This article presents the results of measurements, simulations, and calculations for a commercial microstrip antenna. CST Microwave Studio software was utilized for the modeling. The primary objective was to characterize a commercial antenna using a NanoVNA (a portable Vector Network Analyzer) and subsequently model it in CST Studio. This allowed for verification of the correlation among NanoVNA measurements, computational modeling, and theoretical calculations. Following this, simulations were used to investigate the influence of different dielectric materials on the antenna’s resonant frequency. Through both measurements and simulations, Rogers Corporation RO 3003 was identified as a suitable dielectric for designing a similar microstrip antenna. A strong correlation was observed among the measured, simulated, and calculated values.

TITLE	**CPW Antenna for Satellite Earth Mapping and Radiolocation Systems**
TIME	16:20-16:40 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Marcelo B Perotoni (UFABC, Brazil); Tagleorge Marques Silveira (Instituto de Telecomunicações - IT & Universidade de Aveiro, Portugal); Kenedy Marconi Geraldo Santos (IFBA, Brazil); José Amado (FEDERAL INSTITUTE OF BAHIA & IFBA, Brazil); Crescencio L. R. Neto and Lucas dos Santos Ribeiro (IFBA, Brazil)

ABSTRACT
With the growing demand for devices that rely on satellite-based imaging and radiolocation systems operating across multiple frequency bands, there is a need for antennas capable of ensuring stable communication over a wide spectrum. This work presents the design and experimental validation of an ultra-wideband (UWB) antenna operating from 15 GHz to 25 GHz. The proposed antenna achieves a measured gain of 5.06 dB, demonstrating its potential for integration into next-generation satellite mapping and radiolocation applications.

TITLE	**Dual Wideband Metasurface Based Linear to Circular Polarizer for Transmission Mode**
TIME	16:40-17:00 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Fatima Ghulam (Zhejiang Normal University, China); Hajra Khan (Comsats University Islamabad Abbottabad Campus, Pakistan); Farman Ali Mangi (Shah Abdul Latif University Khairpur, Pakistan); Syed Muzahir Abbas (Macquarie University, Australia)

ABSTRACT
In this paper, a dual wideband metasurface based circular polarizer with high efficiency using complementary split ring resonator is presented to demonstrate the asymmetric transmission of incident x-direction linear polarized (LP) wave into right-hand circularly polarized (RHCP) and left-hand circularly polarized (LHCP) wave at 13.45–14.9 GHz and 14.99–17.21 GHz bands, respectively. The innovative idea of the Fission Transmission of Electromagnetic (FTEM) waves is applied by using double layer to produce pure circularly polarized (CP) wave. Finally, a practical 4 × 4 array is designed which obtained the optimal axial ratio bandwidth of 10.23% and 13.79% at dual bands. The accumulative bandwidth of 24% is obtained across the 12–18 GHz spectrum. The extracted simulated and theoretical results demonstrate the efficiency of structure, in terms of optimal AR, transmission loss, circular dichroism, and wideband characteristics, for practical applicability in advanced polarization conversion applications.

TITLE	**Spiral Blade-Inspired Polarization-Insensitive X-Band FSS for EMI Shielding Applications**
TIME	17:00-17:20 November 6th
VENUE	HUALUXE Hall 3
AUTHORS	Saad Hassan Kiani (Universiti Teknikal malaysia, Melaka, Malaysia); Altaf Ahmed (Universiti Teknikal Malaysia Melaka (UTeM), Malaysia); Muhammad Ikram (American University of Kuwait, Kuwait); Umair Rafique (University of Oulu, Finland); Imran Mohd Ibrahim (Universiti Teknikal Malaysia Melaka, Malaysia); Syed Muzahir Abbas (Macquarie University, Australia)

ABSTRACT
This paper presents the design of an angularly stable, polarization-insensitive bandstop frequency selective surface (FSS) for X-band electromagnetic interference (EMI) shielding applications. The structure features metallic spiral bladeinspired elements enclosed within a ring frame, contributing to its distinctive EM response. The FSS demonstrates bandstop characteristics within the frequency range of 8.73-11.05 GHz, resulting in a fractional bandwidth (FBW) of 23.45%. The bandstop characteristics are primarily governed by the dimensions of the ring and spiral blade elements, optimized through parametric analysis. Furthermore, the transmission performance is evaluated under oblique incidences, demonstrating angular and polarization stability up to a 60-degree angle of incidence for both horizontal (TE) and vertical (TM) polarizations.

TITLE	**Calibration of Simple Transient Electric Field Probe and Circuit-Based Waveform Reconstruction**
TIME	16:20-16:50 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Guangxiao Luo, Yizhe Zhang and Yuhang He (North China Electric Power University (Baoding), China)

ABSTRACT
To improve the transient electric field measurement, this study proposed a circuit-based method to calibrate the simple transient E-field probes and to reconstruct the time-domain waveform. Two probes with different structure were designed: the 1st probe with a partially shielded structure and the 2nd probe with a cylindrical monopole structure. An open strip-line TEM cell and a TEM cell were made for probes calibration respectively. By comparison with the results of the CST MWS and tests, transmission parameter of circuit model including the probes and calibration setups was validated. Then, a time-domain reconstruction method was proposed, the recovered E-field waveform matching the reference result well.

OVERVIEW OF SESSIONS VII

SESSIONS	[SS7] Electromagnetic Compatibility of Integrated Circuits and Components
VENUE	HUALUXE Hall 1
TIME	08:40-12:00 November 7th
SESSION CHAIR	Fayu Wan, Nanjing University of Information Science and Technology, China Anfeng Huang, DeTooLIC Ltd. Technology, China
TECHNICAL TALKS	**From Standard Interpretation to Testing Practice: Exploring the Path to High-Quality CDM Testing (Invited)** *Bingsheng Gao, ESDEMC Technology LLC, China* **Research on the Influence of Signal Integrity of the Test Board on the CAN Transceivers Electromagnetic Interference Test** *Qi Li (National New Energy Vehicles Technology Innovation Center & Automotive Chip Testing and Evaluation Key Laboratory State Administration for Market Regulation, China); Ying Liu (State Administration for Market Regulation, China); Lili Lei (National new Energy Vehicles Technology Innovation Center, China)* **A Broadband Miniature TEM Cell for IC EMC Measurement over 8 GHz** *Chenghao Lan, Yusheng Hu and Yaoquan Ou (Jimei University, China)* **Comparative Study of BSS Algorithms for Noise Source Localization** *Hailing Zhao (Southwest University of Science and Technology, China & Mianyang, China); Bin He (Technology Center XLAB RF Lab Huaqin Technology Co. Ltd., China); Kaiming Ding, Haiying Wang and Shengjun Liu (Huaqin Technology Co. Ltd., China)* **Exploration of the Relationship Between Copper Foil Microstructure and Etching Behavior on PCB Signal Integrity** *Changdong Gu (Zhejiang Huanergy, China)* **Charged Device Model Electrostatic Discharge Sensitivity Tester Based on 3D Vision** *Minfeng Xia, Jichen Wei, Liyuan Shi, Jiawen Chen and Fayu Wan (Nanjing University of Information Science and Technology, China)* **Integrated Coaxial Resonator for Reconfigurable Passive Intermodulation Testing** *Min Liang, Xiong Chen and Bin Han (Xi'an Jiaotong University, China)* **Tunable Phase Shifter Using Monolithic Sliding Triple-Line Structure** *Yuhan Liu, Xiong Chen and Zhou Han (Xi'an Jiaotong University, China)* **A Method for Generating Approximately Non-Diffracting Möbius Rings** *Yueyi Yuan, Na Ri, Yuxiang Wang and Kuang Zhang (Harbin Institute of Technology, China)*

TITLE	**From Standard Interpretation to Testing Practice: Exploring the Path to High-Quality CDM Testing (Invited)**
TIME	08:40-09:00 November 7th
VENUE	HUALUXE Hall 1
AUTHOR	Bingsheng Gao, ESDEMC Technology LLC, China

ABSTRACT

This presentation addresses the key challenges faced in Charged Device Model (CDM) testing, including inconsistent understanding of standards, poor test repeatability, and difficulties in adapting to non-standard or irregular device types. It systematically reviews core industry standards such as JEDEC/ESDA JS-002, providing an in-depth analysis of their technical evolution, methodological differences, and calibration requirements to establish a clear framework for proper standard implementation. On the practical side, an innovative RP-CCDM testing method is proposed, along with validated solutions tailored for complex scenarios such as irregular packages and wafer-level devices. By combining standard interpretation with practical innovation, this work aims to enable more reliable, accurate, and high-quality CDM testing.

BIOGRAPHY

Bingsheng Gao received his MSc of Physical electronics, specializing in ESD and EMC, from the School of Information Engineering, Wuhan University of Technology. He is currently working as a applications engineer at ESDEMC Technology Co., Beijing Branch. Over the years, he has been mainly engaged in device level and system level ESD and EMC test research, as well as technical support for such test equipment.

TITLE	**Research on the Influence of Signal Integrity of the Test Board on the CAN Transceivers Electromagnetic Interference Test**
TIME	09:00-09:20 November 7th
VENUE	HUALUXE Hall 1
AUTHORS	Qi Li (National New Energy Vehicles Technology Innovation Center & Automotive Chip Testing and Evaluation Key Laboratory State Administration for Market Regulation, China); Ying Liu (State Administration for Market Regulation, China); Lili Lei (National new Energy Vehicles Technology Innovation Center, China)

ABSTRACT

In this paper, we have analyzed the test method of EMC evaluation of CAN transceivers based on lEC62228-3, elaborate on the test configuration, test circuits, test board of electromagnetic interference test. And performed the electromagnetic interference test for the same automotive CAN transceiver using different test boards, research on the influence of signal integrity of the test board on the CAN transceivers electromagnetic interference test, and some suggestions for the design of the test board were provided.

TITLE	**A Broadband Miniature TEM Cell for IC EMC Measurement over 8 GHz**
TIME	09:20-09:40 November 7th
VENUE	HUALUXE Hall 1
AUTHORS	Chenghao Lan, Yusheng Hu and Yaoquan Ou (Jimei University, China)

ABSTRACT
The upper limited operating frequency of the traditional transverse electromagnetic (TEM) cell for integrated circuit (IC) electromagnetic compatibility (EMC) test is only about 1 GHz. With the ever-increasing frequency of IC or other electronic devices, higher operating frequency TEM cell is required. In this paper, an modified miniature TEM cell as well as the measuring method are presented. The overall structure of the proposed miniature TEM cell is similar to the traditional TEM cell, but its bottom has a rectangular aperture whose size is of the same order of magnitude as the device under test (DUT), or is completely open. The miniature TEM cell is directly covered on the IC of the working printed circuit board (PCB) for EMC testing. The design of the measuring device is described in detail, and whose electromagnetic performances are analyzed by numerical method. The experimental verification is carried out by making a prototype. Since the size of the TEM cell is significantly reduced, its operating frequency can reach above 8 GHz. In addition, there is no need to make a special PCB board, and online measurement is realized.

TITLE	**Comparative Study of BSS Algorithms for Noise Source Localization**
TIME	10:00-10:20 November 7th
VENUE	HUALUXE Hall 1
AUTHORS	Hailing Zhao (Southwest University of Science and Technology, China & Mianyang, China); Bin He (Technology Center XLAB RF Lab Huaqin Technology Co. Ltd., China); Kaiming Ding, Haiying Wang and Shengjun Liu (Huaqin Technology Co. Ltd., China)

ABSTRACT
With the increasing operating speeds of electronic devices and the growing density of electronic systems, a rising number of potential noise sources may emerge. Blind Source Separation (BBS), which separates mixed noisy signals to transform conventional qualitative analysis into quantitative and traceable solutions, shows broad application prospects. Therefore, this paper compares several common BBS algorithms through simulation tests, verifies their performance differences, and thereby provides a reference for selecting suitable algorithms in practical Electromagnetic Interference (EMI) optimization tasks.

TITLE	**Exploration of the Relationship Between Copper Foil Microstructure and Etching Behavior on PCB Signal Integrity**
TIME	10:20-10:40 November 7th
VENUE	HUALUXE Hall 1
AUTHORS	Changdong Gu (Zhejiang Huanergy, China)

ABSTRACT
The signal integrity of the conductor for high frequency and high-speed digital applications requires copper foils with lower profiles and without magnetic elements. As well as the copper foil profile and surface chemistry, some manufacturing processes, may also influence the signal integrity performances of the end product. Particularly, the crystallographic orientations and grain boundaries of the copper foils would play important roles in manipulating surface morphologies in PCB etching, which further influences the signal integrity of the conductor in HDIs. Herein, low profile copper foils with tunable crystallographic structures and surface morphologies were fabricated by the copper foil manufacturing industry and received the same and routine manufacturing processes in CCL and PCB sections. Thus, the impact of the microstructures of copper foil on the signal integrity was finally obtained by experimental investigations

TITLE	**Charged Device Model Electrostatic Discharge Sensitivity Tester Based on 3D Vision**
TIME	10:40-11:00 November 7th
VENUE	HUALUXE Hall 1
AUTHORS	Minfeng Xia, Jichen Wei, Liyuan Shi, Jiawen Chen and Fayu Wan (Nanjing University of Information Science and Technology, China)

ABSTRACT
An electrostatic discharge (ESD) sensitivity tester for charged device model (CDM) is developed in this paper. The tester can simulate the charging and discharging of CDM ESD, in order to measure the discharge current. A 3D vision module is integrated and used to observe the pin distribution of the device under test (DUT) during real-time testing, enabling recognition, positioning, and automated measurement of sub millimeter sized pins. The discharge signals of GHz level can be transmitted without distortion and shown on an oscilloscope. The robustness of the DUT to ESD can be evaluated by analyzing the discharge signal and the operation state of the DUT after discharge.

TITLE	**Integrated Coaxial Resonator for Reconfigurable Passive Intermodulation Testing**
TIME	11:00-11:20 November 7th
VENUE	HUALUXE Hall 1
AUTHORS	Min Liang, Xiong Chen and Bin Han (Xi'an Jiaotong University, China)

ABSTRACT
A coaxial resonator model for Passive Intermodulation (PIM) testing was established in this paper. The model incorporates a probe inserted into the resonator, and a stepped coaxial line is used as the probe to enable application across a wider frequency range. The proposed model features multiple resonance points around the frequencies of 2.62 GHz and 2.69 GHz, resulting in a return loss better than 20 dB within this frequency range. This effectively prevents interference from reflected signals on incident signals, making the model suitable for full-band testing of Band 41.

TITLE	**Tunable Phase Shifter Using Monolithic Sliding Triple-Line Structure**
TIME	11:20-11:40 November 7th
VENUE	HUALUXE Hall 1
AUTHORS	Yuhan Liu, Xiong Chen and Zhou Han (Xi'an Jiaotong University, China)

ABSTRACT
This paper introduces a mechanically tunable phase shifter employing a monolithic sliding triple-line structure. By physically translating the central conductor, the design achieves continuous phase shift in a fully passive planar architecture, overcoming the power and linearity limitations of semiconductor-based approaches. Simulation results validate the model, demonstrating a continuous phase shift up to 150° within the 1.6–1.8 GHz band. This work presents a practical solution for high-power applications, with future enhancements targeting integrated filtering for improved performance.

TITLE	**A Method for Generating Approximately Non-Diffracting Möbius Rings**
TIME	11:40-12:00 November 7th
VENUE	HUALUXE Hall 1
AUTHORS	Yueyi Yuan, Na Ri, Yuxiang Wang and Kuang Zhang (Harbin Institute of Technology, China)

ABSTRACT

This paper presents a method for generating approximately non-diffracting polarized Möbius rings, which remain stable over a propagation distance from 1λ to 100λ, with a transmission efficiency exceeding 60%. The designed metasurface focuses the co-polarized component of the incident left-hand circularly polarized (LCP) beam, while imparting orbital angular momentum with a topological charge of m = -1 to the cross-polarized component.

OVERVIEW OF SESSIONS VIII

SESSIONS	[SS8] Advanced SI Modeling, Design, and Testing Techniques
VENUE	HUALUXE Hall 3
TIME	08:40-12:00 November 7th
SESSION CHAIR	Lei Deng, LinkE Technologies, China Si-Ping Gao, Nanjing University of Aeronautics and Astronautics, China
TECHNICAL TALKS	**A de-Embedding Method for High-Speed Single-Ended Signals with Three-Port Test Fixture** *Rui Miao, Tao Wei and Xiuqin Chu (Xidian University, China); Jun Wang (Xidian University, China); Rui Chen, Yuhao Huang and Aobo Li (Xidian University, China)* **A Novel Method for Calculating Crosstalk de-Embedding Transfer Function in High-Speed Link** *Rui Chen and Yuhao Huang (Xidian University, China); Jun Wang (Xidian University, China); Rui Miao, Aobo Li and Xiuqin Chu (Xidian University, China)* **Novel Methodology for Electrical Performance Characterization of High-Speed Raw Cables Under Thermal Stress** *Jimmy Hsu (Intel, Taiwan); Huafang Ju (Intel (China) Ltd., China); Ryan Chang (Intel Technology Asia Pte. Ltd., Taiwan)* **Delay Matters: Enhancing S-Parameter Macromodeling Accuracy** *Chenxi Liu, Qi Liu and Yajun Chen (DeTooLIC Ltd. Technology, China); Yi Chen (ZTE Corporation, China); Yanwu Wang and Zhifei Xu (DeTooLIC Ltd. Technology, China)* **Connectors for 400 Gbps-per-Lane Links: Challenges and Design Directions** *Lei Deng (LinkE Technologies, China)* **Twinax Cables at 448 Gb/s: Challenges and Solutions** *Lei Deng (LinkE Technologies, China)* **2.4 GHz Wideband Tunable Impedance Matching Network** *Bin Han, Xiong Chen and Zhou Han (Xi'an Jiaotong University, China)* **Implementation of an Adaptive DFE Algorithm** *Wenbo Zhang (Avic Xi'an Aeronautics Computing Technique Research Institute', China); Tingting Liu, Yang Liu, Xuanyu Wang, Siyuan Li, Sichao Guo, Xiaozhe Han, Yaqi Li, Yiqiong Pang and Ying Zhu (Avic Xi'an Aeronautics Computing Technique Research Institute, China)* **Research on GMSL Testing Technology in Multi-Physical Field Environments** *Yuxu Huo (AVIC Xi'an Aeronautics Computing Technique Research Institute, China); Zichun Zhang (Xi'an Aeronautics Computing Technique Research Institute, China); Chuangye Guo (AVIC Xi'an Aeronautics Computing Technique Research Institute, China); Tingting Liu (Avic Xi'an Aeronautics Computing Technique Research Institute, China)*

TITLE	**A de-Embedding Method for High-Speed Single-Ended Signals with Three-Port Test Fixture**
TIME	08:40-09:00 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Rui Miao, Tao Wei and Xiuqin Chu (Xidian University, China); Jun Wang (Xidian University, China); Rui Chen, Yuhao Huang and Aobo Li (Xidian University, China)

ABSTRACT

As the data rates of DDR memory continue to increase, the test interposer is frequently used in the DDR system measurement. Therefore, a de-embedding method must be applied to reconstruct the actual signals at DRAM pins. A novel de-embedding method for high-speed single-ended signals with the three-port test fixture is proposed based on S-parameter and transfer function. The test scenario of DDR with an interposer is first modelled by S-parameters, especially modelling the interposer as a three-port network, and then the de-embedding transfer function is derived through the signal flow graph method. The effectiveness and accuracy of the method are validated by measurements.

TITLE	**A Novel Method for Calculating Crosstalk de-Embedding Transfer Function in High-Speed Link**
TIME	09:00-09:20 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Rui Chen and Yuhao Huang (Xidian University, China); Jun Wang (Xidian University, China); Rui Miao, Aobo Li and Xiuqin Chu (Xidian University, China)

ABSTRACT

The frequency of high-speed links is continuously increasing, while in modern equipment, the influence of crosstalk in measurement techniques cannot be ignored. A new methodology is proposed for accurately evaluating the impact of crosstalk in de-embedding techniques for high-speed link testing. The proposed method accurately calculates the de-embedded transfer function under the influence of crosstalk, and reconstructs the waveform at the point of interest based on signals at the test points of high-speed link channels. It also reveals the calculation method for both the transmitted signal and the crosstalk signal in the time and frequency domains. For validation, the results are compared with measured data, confirming the method's accuracy.

TITLE	**Novel Methodology for Electrical Performance Characterization of High-Speed Raw Cables Under Thermal Stress**
TIME	09:20-09:40 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Jimmy Hsu (Intel, Taiwan); Huafang Ju (Intel (China) Ltd., China); Ryan Chang (Intel Technology Asia Pte. Ltd., Taiwan)

ABSTRACT
In recent years, the continuous increase in interface speeds within data centers has led to the widespread adoption of high-speed copper cables. Concurrently, as power consumption in data centers escalates, designers are increasingly concerned about cable loss across broader temperature ranges. It is relatively straightforward to simulate the insertion loss at room temperature, but accurately estimating loss at elevated temperatures is more complex and resource-intensive. This paper proposes a novel methodology for characterizing the electrical performance of high-speed raw cables under thermal stress. The approach provides essential groundwork and support for addressing the challenges posed by PCIe 6.0, particularly regarding the thermal sensitivity of cable electrical properties. The goal is to enable engineers to accurately and reliably estimate cable loss under real-world temperature conditions in data center environments, thereby supporting PCIe 6.0 applications and future high-speed interconnect technologies.

TITLE	**Delay Matters: Enhancing S-Parameter Macromodeling Accuracy**
TIME	10:00-10:20 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Chenxi Liu, Qi Liu and Yajun Chen (DeTooLIC Ltd. Technology, China); Yi Chen (ZTE Corporation, China); Yanwu Wang and Zhifei Xu (DeTooLIC Ltd. Technology, China)

ABSTRACT
In high-speed circuit design, S-parameters are critical for accurately characterizing the frequency-domain behavior of interconnect channels. However, their inherent limitation—inability to support efficient transient or nonlinear simulations — necessitates conversion into equivalent SPICEcompatible models. To address this, this paper proposes a modified Vector Fitting (VF) process that separates the delay term from the fitting procedure. This modification not only accelerates the convergence of the fitting process but also enhances model accuracy by enabling effective order reduction. Validation results show that while some conventional Sparameter-derived models failed to complete transient simulations in HSPICE, the SPICE model generated via the proposed S2Spice method achieved efficient simulation execution with high accuracy.

TITLE	**Connectors for 400 Gbps-per-Lane Links: Challenges and Design Directions**
TIME	10:20-10:40 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Lei Deng (LinkE Technologies, China)

ABSTRACT
The rapid growth of artificial intelligence (AI) continues to drive higher interconnect bandwidth demand. 200 Gbps-per-lane PAM4 links have been deployed in leading AI systems, and the industry is now moving toward 400 Gbps-perlane and beyond. At these data rates, the physical dimensions of connectors become electrically significant, introducing resonances, crosstalk, and impedance discontinuities that degrade signal integrity (SI). This paper reviews the primary limitations of 400 Gbps-per-lane connectors and presents recent emerging design innovations and strategies for next-generation high-speed interconnects.

TITLE	**Twinax Cables at 448 Gb/s: Challenges and Solutions**
TIME	10:40-11:00 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Lei Deng (LinkE Technologies, China)

ABSTRACT
Electrical links at 448 Gb/s are increasingly constrained by cable insertion loss, higher-order-mode (HOM) excitation, and intra-pair skew. This paper reviews recent advances in twinax cables and, for 448 Gb/s PAM4 lanes with Nyquist near 112 GHz, analyzes these constraints and their design implications. Design approaches are presented to reduce loss, raise the HOM onset frequency, and mitigate skew to meet end-to-end compliance.

TITLE	**2.4 GHz Wideband Tunable Impedance Matching Network**
TIME	11:00-11:20 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Bin Han, Xiong Chen and Zhou Han (Xi'an Jiaotong University, China)

ABSTRACT
This paper designs and implements a 2.4 GHz tunable impedance matching network based on a four-branch microstrip line structure. The system uses varactor diodes as tunable components, achieving continuous impedance tuning by adjusting the bias voltage. A hybrid matching structure combining microstrip lines, inductors, and capacitors is employed to achieve wide impedance matching while maintaining good matching characteristics. The entire network is simulated using electromagnetic and circuit co-simulation in software, and the results show that the matching network operates within a real part range of 70–120 Ω and an imaginary part range of 20–60 Ω. In the 2.3–2.5 GHz frequency band, the network achieves S11 less than -20 dB with a maximum bandwidth of 323 MHz, effectively enabling dynamic matching for complex impedance loads.

TITLE	**Implementation of an Adaptive DFE Algorithm**
TIME	11:20-11:40 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Wenbo Zhang (Avic Xi'an Aeronautics Computing Technique Research Institute', China); Tingting Liu, Yang Liu, Xuanyu Wang, Siyuan Li, Sichao Guo, Xiaozhe Han, Yaqi Li, Yiqiong Pang and Ying Zhu (Avic Xi'an Aeronautics Computing Technique Research Institute, China)

ABSTRACT
DFE (Decision Feedback Equalizer) is one of the key technologies for addressing issues such as reflection, Inter-Symbol Interference (ISI), and impedance discontinuity in the channel of SerDes systems. Its core principle is to eliminate the ISI of the current symbol by feeding back the decision results of previous symbols, and it complements the Continuous Time Linear Equalization (CTLE). Meanwhile, adaptive algorithms (e.g., LMS/RLS algorithms) can be used to dynamically adjust the DFE tap coefficients according to the channel characteristics. This paper mainly discusses and analyzes the principle and algorithm implementation of the Decision Feedback Equalizer (DFE). To verify the accuracy of the equalization algorithm, a comparison is conducted with the equalization algorithm in commercial simulation software. The difference between the two is very small, which proves that the equalization algorithm implemented in this paper is accurate and reliable.

TITLE	**Research on GMSL Testing Technology in Multi-Physical Field Environments**
TIME	11:40-12:00 November 7th
VENUE	HUALUXE Hall 3
AUTHORS	Yuxu Huo (AVIC Xi'an Aeronautics Computing Technique Research Institute, China); Zichun Zhang (Xi'an Aeronautics Computing Technique Research Institute, China); Chuangye Guo (AVIC Xi'an Aeronautics Computing Technique Research Institute, China); Tingting Liu (Avic Xi'an Aeronautics Computing Technique Research Institute, China)

ABSTRACT

With the automotive industry moving toward a new era of intelligence, GMSL technology is widely applied in autonomous vehicle platforms. This paper primarily studies GMSL interface testing technology. First, the GMSL interface protocol and transmission mechanism were thoroughly studied, and the current application status of GMSL interface technology was investigated. Second, a high-speed serial signal testing solution based on the GMSL interface was built using the Tektronix DPO71254X oscilloscope software and hardware, as well as its high and low-temperature probes, and Adaptive Separation Algorithm was employed for secondary processing of experimental data to extract complete forward high-speed signals. Subsequently, the impact of temperature on physical layer signals was tested under different temperature conditions. Finally, the effects of temperature and transmission link were compensated using the CTLE and DFE equalization algorithms supported by GMSL Generation 2. Experimental results demonstrate that the complete set of technical methods proposed in this paper provides a feasible solution for GMSL bus signal testing and also offers guidance for the signal optimization design at the receiving end, with certain reference value for both academic research and production applications.

PANEL DISCUSSION I

TOPIC	**Addressing the Ever-Growing Challenges in High-Speed Interconnect Designs in the AI Era: EDA Perspectives**
TIME	10:20 – 12:00, November 6th
VENUE	**Liren Hall 2（里仁厅二）**
PANEL CHAIR	Bo Pu, TPC chair, International Workshop on Advanced Interconnects (WAI)
INVITED PANELIST	Stanley Zheng, EDA² Michael Liu, Empyrean Technology Haisan Wang, Cadence Kefei Zhang, Semitronix Yin Sun, DeTooLIC Technology Ming Zhou, Dassault Systemes Haidong Zhang, NineCube Xiuguo Jiang, Keysight

KEY TOPICS INCLUDE:

- Global and local Market Demands: EDA of high-speed and high bandwidth interconnects for Chiplet, data centers, AI systems, and supercomputing infrastructure.
- Innovative Solutions and Future Trends: Exploring cutting-edge solutions and technological advancements to meet the industry's demands.

BIO OF PANEL CHAIR

Bo Pu, TPC chair, International Workshop on Advanced Interconnects (WAI)

Dr. Bo Pu is the TPC chair of WAI. He was a Staff Engineer in charge of design methodology for AP, SerDes, HBM2/2E/3, DDR5 and GDDR6 from 14nm to 3nm as well as responsible for collaborating with Cadence and ANSYS in Samsung Semiconductor HQ, Korea. Then he joined Missouri University of Science and Technology, MO, USA as an assistant research professor. Currently He is the VP of DeTooLIC Technology. He published over 50 technical papers and holds 15 patents about high speed links and 2.5D/3D ICs.

He is the TPC chair and Member of the IEEE WAI, IEEE EMCS, IEEE APEMC, ISEMC and ACES. He was also awarded the 2014 URSI Young Scientists Award, 2022 APEMC Outstanding Young Scientists Award, and the 2020, 2021 Distinguish reviewer of IEEE Transactions on EMC, 2023 Outstanding Associate Editor of IEEE Access. Dr. Pu is a recipient of the Technical Achievement Award from IEEE EMC Society.

BIOS OF INVITED PANELIST

Stanley Zheng, EDA²

Stanley Zheng graduated from the Department of Computer Science at Fudan University and holds an MBA from Macau University of Science and Technology. He has served as Senior Engineer at Inventec, Engineering Manager at Phoenix Technologies, Technical Support Manager/Strategy Director at Intel, and Director of Semiconductor Industry Development at Huawei. His work experience spans OS development, BIOS/EFI development, chip technical support, marketing, ecosystem promotion, IP strategy, 7nm chip product development, and industry development. He is the only person in Intel China ever served as a global chip leader. He currently serves as the Director of External Cooperation Committee and Chief of Standards at EDA².

Michael Liu, Empyrean Technology

Michael Liu is the senior product director of Empyrean Technology. He has more than 10 years of experience in ASIC chip design, manufacturing, and packaging EDA software product development and management, focusing on the planning, development, and promotion of EDA products. He helps Empyrean build up a mature Analog/Mixed-Signal design flow, and expand it to the fields of other full custom design such as flat panel display, signal chain, memory, RF and optoelectronics. He is building a reliability design methodology for design-manufacturing collaboration and a PPAC-oriented design-manufacturing packaging collaborative design solution. The solutions are widely adopted by national and international leading design houses.

Haisan Wang, Cadence

Haisan Wang is an AE director from Cadence Multi-Physics System Analysis (MSA) service AE team. He mainly focuses on performing high performance chip system design by co-design and co-simulation technology. Prior to joining Cadence, he worked at Sigrity and Huawei.

Kefei Zhang, Semitronix

Kefei Zhang has over 20 years of work experience in the field of chip design services and IP/EDA. Having worked in various positions such as design, product planning, and marketing promotion in multiple IPO companies.

He has successfully planned multiple video and IoT chips. He has rich experience in product management and technical marketing within the fields of chiplet, high- performance SoC, and IP.

Yin Sun, DeTooLIC Technology

Dr. Yin Sun heads the Product and Technology departments at Ningbo Detoolic Technology Co., Ltd. She holds a Ph.D. from Missouri University of Science and Technology, an M.S. from The Hong Kong University of Science and Technology, and a B.S. from Fudan University. Her research focuses on signal and power integrity in high-speed integrated circuit chips and packaging, as well as electromagnetic compatibility.

Ming Zhou, Dassault Systemes

Zhou Ming earned his Master of Engineering degree from Harbin Institute of Technology. He has long specialized in electromagnetic field simulation technology research and possesses rich engineering application experience, providing CST simulation guidance and technical support to major clients in the high-tech and automotive industries.

Haidong Zhang, NineCube

Zhang Haidong is currently leading FEM Electromagnetic and Thermal Product line at NineCube. He has over 10 years of specialized experience in electromagnetic simulation tools. He obtained a master's degree from Shanghai Jiao Tong University in 2012.

Xiuguo Jiang, Keysight

Xiuguo Jiang is the Great China EDA SE&CSM Manager at Keysight Technologies, where he focuses on Signal Integrity, Power Integrity, and EMC. He has more than 15 years of experience in Hardware and Signal integrity. Prior to joining Keysight Technologies, Xiuguo worked on system and component design. In recent years, he has been focused on the modeling of PCB, Package, and Components as well as some challenges of signal integrity and power integrity. He is the author of over 5 books on SI, PI, and EE. He operates WeChat Official Account <Signal Integrity> as a founder. The follower is more than 60k. He holds 1 Chinese patent. He published 4 papers.

PANEL DISCUSSION II

TOPIC	**Data Center High-Speed Interconnect in the AI Era: Part I - Innovations in Materials and Manufacturing**
TIME	13:20 – 14:20, November 6th
VENUE	**Liren Hall 2（里仁厅二）**
PANEL CHAIR	Harrison Xue， Senior SI Architect, Lenovo
INVITED PANELIST	Jiangqi He, NINGBO Everstrong Technology Co., Ltd. Loong Jin, LUXSHARE-TECH Technology Co., Ltd. Fazhi Liu, Huaqin Technology Co., Ltd. Jinshan Ma, IEIT Systems Jeff Pan, Zhejiang Huanergy Co., Ltd. Xiangnan Sun, Starsmicrosystem Co., Ltd. Yanwu Wang, DeTool Technology Co., Ltd. Kepeng Zhai, Kinwong Electronics Co., Ltd.

BIO OF PANEL CHAIR

Harrison Xue, Lenovo

Harrison Xue Fei is a senior SI architecture in Lenovo CSP. He was a Technical Lead in Intel. He works on signal integrity of high-speed interconnect in server, storage, data center systems and desktop laptop. He published 20+ technical papers in technical conference and at Intel. He received his bachelor and master's degrees in UESTC, Chengdu, China in 2002 and 2005 respectively.

BIOS OF INVITED PANELIST

Jiangqi He, NINGBO Everstrong Technology Co., Ltd.

Dr. Jiangqi was an intel Principal Engineer on advanced packaging, power integrity, power delivery and associated server hardware engineering. He was the founder and the director of hardware research lab and technical vice president for Huawei's North America research institute. From 2019 he started up NINGBO Everstrong technology which is focusing on advanced materials for advanced packaging and high-speed interconnect. Dr. He published more than 50 technical papers and owns more than 80 U.S. patents. His recent interest is new materials to meet AI needs.

Loong Jin, LUXSHARE-TECH Technology Co., Ltd.

Loong Jin has over 15 years of professional experience in the high-speed connector and cable assembly industry, having planned and led the development of multiple product lines including SSIO, HSIO, and BP. He also possesses extensive experience in the application and practice of interconnect solutions.

Fazhi Liu, Huaqin Technology Co., Ltd.
Fazhi Liu has over 10 years of experience architecting and de-risking high-speed digital systems for data-centric applications. Provides technical leadership across the entire product lifecycle, from initial system architecture and material selection to production bring-up and failure analysis. Focused on the design and validation of PCIe Gen5/6 and 112G/224G PAM4 SerDes channels, alongside robust Power Integrity implementation to ensure system-level performance.

Jinshan Ma, IEIT Systems
Jinshan Ma, specializing in the server industry, leads upstream and downstream product planning and R&D, driving technology implementation and product iteration. Possesses extensive cross-domain technical expertise, having previously worked at companies such as Moore threads, Sugon, and Zhongsheng Hongxin. Responsible for core tasks including GPU chip product planning, supercomputer system architecture design, and CPU chip system platform design, with comprehensive technical vision and practical capabilities spanning from chips and servers to supercomputing systems.

Jeff Pan, Zhejiang Huanergy Co.,Ltd.
Jeff Pan serves as the President of Zhejiang Huanergy Co., Ltd., which was founded in 2017 and the company specializes in high-end copper foil research and production in the electronics and lithium-ion battery industries. Jeff holds an MBA degree from the Fuqua School of Business, Duke University.

Xiangnan Sun, Starsmicrosystem Co., Ltd.
Xiangnan Sun is responsible for the packaging R & D and mass production operation of all the company's products. In the R&D part, he collaborates with the design team and is mainly in charge of the packaging and system SI of all the company's products, including package design, package and system SIPI simulation, thermal simulation, stress simulation, and package engineering. He is also responsible for the introduction of the company's chip packaging from NPI to mass production. In the operation part, he is mainly responsible for the mass - production shipment of all the company's products, production planning, production management, account reconciliation, and ERP system maintenance.

Yanwu Wang, DeTool Technology Co.,Ltd.
Yanwu Wang focuses on EDA solutions for signal and power integrity design, optimization, and system solutions. He has over 20 years of experience in high-speed SerDes and DDR design for computer and server products. Before joining Detool, he was responsible for high-speed system design and product development at multiple companies.

Kepeng Zhai, Kinwong Electronics Co., Ltd.
Graduated from Guilin University of Electronic Technology with a Bachelor's degree in Communication Engineering in 2015. Previously worked at a leading communication design company, responsible for the design and simulation of RF circuits and antennas for consumer electronic products. He joined in Kinwong in 2020 and be employed in a Senior Manager of R&D. Responsible for electromagnetic field analysis and design optimization of high-frequency and high-speed PCBs. Main research areas including high-speed interconnection modeling, simulation and measurement. This includes PCB material selection, stack-up design, material parameter extraction and design simulation verification.

PANEL DISCUSSION III

TOPIC	**Data Center High-Speed Interconnect in the AI Era: Part II - Architecturing the Interconnect for the Future**
TIME	14:20 – 15:20, November 6th
VENUE	**Liren Hall 2（里仁厅二）**
PANEL CHAIR	Harrison Xue, Lenovo
INVITED PANELIST	Lei Deng, Zhuhai LinkE Technology Co., Ltd. Jiangqi He, NINGBO Everstrong Technology Co., Ltd. Loong Jin, LUXSHARE-TECH Technology Co., Ltd. Fazhi Liu, Huaqin Technology Co., Ltd. Jinshan Ma, IEIT Systems Anbing Sun, Ruijie Networks Xiangnan Sun, Starsmicrosystem Co., Ltd. Yanwu Wang, DeTool Technology Co., Ltd. Kepeng Zhai, Kinwong Electronics Co., Ltd.

BIO OF PANEL CHAIR

Harrison Xue, Lenovo

Harrison Xue Fei is a senior SI architecture in Lenovo CSP. He was a Technical Lead in Intel. He works on signal integrity of high-speed interconnect in server, storage, data center systems and desktop laptop. He published 20+ technical papers in technical conference and at Intel. He received his bachelor and master's degrees in UESTC, Chengdu, China in 2002 and 2005 respectively.

BIOS OF INVITED PANELIST

Lei Deng, Zhuhai LinkE Technology Co., Ltd.

Deng Lei has over 15 years of R&D experience in high-speed interconnects, antenna technology and high-performance RF system design. Currently, he is leading the team to develop cutting-edge solutions for next-generation connectivity. He holds a bachelor's and master's degree from Huazhong University of Science and Technology.

Jiangqi He, NINGBO Everstrong Technology Co., Ltd.

Dr. Jiangqi was an intel Principal Engineer on advanced packaging, power integrity, power delivery and associated server hardware engineering. He was the founder and the director of hardware research lab and technical vice president for Huawei's North America research institute. From 2019 he started up NINGBO Everstrong technology which is focusing on advanced materials for advanced packaging and high-speed interconnect. Dr. He published more than 50 technical papers and owns more than 80 U.S. patents. His recent interest is new materials to meet AI needs.

Loong Jin, LUXSHARE-TECH Technology Co., Ltd.

Loong Jin has over 15 years of professional experience in the high-speed connector and cable assembly industry, having planned and led the development of multiple product lines including SSIO, HSIO, and BP. He also possesses extensive experience in the application and practice of interconnect solutions.

Fazhi Liu, Huaqin Technology Co., Ltd.

Fazhi Liu has over 10 years of experience architecting and de-risking high-speed digital systems for data-centric applications. Provides technical leadership across the entire product lifecycle, from initial system architecture and material selection to production bring-up and failure analysis. Focused on the design and validation of PCIe Gen5/6 and 112G/224G PAM4 SerDes channels, alongside robust Power Integrity implementation to ensure system-level performance.

Jinshan Ma, IEIT Systems

Jinshan Ma, specializing in the server industry, leads upstream and downstream product planning and R&D, driving technology implementation and product iteration. Possesses extensive cross-domain technical expertise, having previously worked at companies such as Moore threads, Sugon, and Zhongsheng Hongxin. Responsible for core tasks including GPU chip product planning, supercomputer system architecture design, and CPU chip system platform design, with comprehensive technical vision and practical capabilities spanning from chips and servers to supercomputing systems.

Anbing Sun, Ruijie Networks

Sun Anbing has more than 15 years of experience in PCB/SI and is currently focused on the hardware system architecture design and new technology research of the next-generation data center switche

Xiangnan Sun, Starsmicrosystem Co., Ltd.

Xiangnan Sun is responsible for the packaging R & D and mass production operation of all the company's products. In the R&D part, he collaborates with the design team and is mainly in charge of the packaging and system SI of all the company's products, including package design, package and system SIPI simulation, thermal simulation, stress simulation, and package engineering. He is also responsible for the introduction of the company's chip packaging from NPI to mass production. In the operation part, he is mainly responsible for the mass - production shipment of all the company's products, production planning, production management, account reconciliation, and ERP system maintenance.

Yanwu Wang, DeTool Technology Co.,Ltd.

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Kepeng Zhai, Kinwong Electronics Co., Ltd.

Graduated from Guilin University of Electronic Technology with a Bachelor's degree in Communication Engineering in 2015. Previously worked at a leading communication design company, responsible for the design and simulation of RF circuits and antennas for consumer electronic products. He joined in Kinwong in 2020 and be employed in a Senior Manager of R&D. Responsible for electromagnetic field analysis and design optimization of high-frequency and high-speed PCBs. Main research areas including high-speed interconnection modeling, simulation and measurement. This includes PCB material selection, stack-up design, material parameter extraction and design simulation verification.

PANEL DISCUSSION IV

TOPIC	**Trends in Smart Devices and Challenges Related to Electromagnetic Interference in the AI Era**
TIME	15:40 – 16:40, November 6th
VENUE	**Liren Hall 2（里仁厅二）**
PANEL CHAIR	Anfeng Huang, DeTooLIC Technology
INVITED PANELIST	Yiqiang Zhang, VIVO; Kaixiang Zhu, HONOR; Kaiming Ding, Huaqin Technology Co., Ltd.; Wenju Sheng, Huawei Device Co., Ltd.; Chengming Wang, Xiaomi;

BIO OF PANEL CHAIR

Anfeng Huang, DeTooLIC Technology

Anfeng Huang (Member, IEEE) received the B.E. and M.S. degrees in electrical engineering from Xidian University, Shaanxi, China, in 2014 and 2017, respectively, and the Ph.D. degree in electrical engineering from the Missouri University of Science and Technology, Rolla, MO, USA, in 2022. He is currently with Detooltech, Ningbo, China. His current research interests include EMI in power electronics, magnetic material characterization, and advanced measurement techniques.

BIOS OF INVITED PANELIST

Yiqiang Zhang, VIVO

Over 20+ years EMC design experience in network equipment and mobile terminals

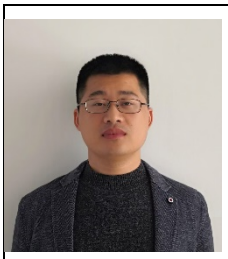
- vivo software Technology co., Ltd., EMC expert, started 2019
- TD Tech Communications co.,Ltd., EMC expert 2016-2019
- Nokia China, EMC expert, 2011-2015
- H3C, EMC design, 2005-2011

Kaixiang Zhu, HONOR

Kaixiang Zhu received the B.S. degree and the Ph.D. degree from Beihang University, Beijing China, in 2013 and 2019. He is currently a Senior Engineer with Honor Device, working towards RF interterence, susceptibility of multimedia module and other EMI problems in terminal products.

Kaiming Ding, Huaqin Technology Co., Ltd.

Kaiming Ding is currently employed at Huaqin Technology Co., Ltd. as a Senior Advanced Engineer, with over 10 years of experience in EMC engineering projects. He is responsible for technical pre-research in the EMC direction at the Group Technology Center and has recently focused on the research and resolution of radio frequency interference, immunity, and nonlinear issues in the consumer electronics field.



Wenju Sheng, Huawei Device Co., Ltd.

Sheng Wenju, a graduate of Wuhan Institute of Technology, is the Director of the High-Frequency & High-Speed Capability Center and the Chief SI & PI Expert in the Terminal Interconnection Department at Huawei Device Co., Ltd. He is also recognized as a Level 7 Expert in Device Board-Level Hardware and Process. He specializes in Signal Integrity (SI) and Power Integrity (PI) engineering for mobile phones, tablets, and PCs in challenging scenarios characterized by high density, high bandwidth, strong interference, and low power consumption.

Chengming Wang, Xiaomi

Chengming Wang received his B.S. (2018) and M.S. (2021) degrees in Information Science and Electronic Engineering from Zhejiang University. He is currently a Senior Engineer at the Simulation Department of Xiaomi Corporation, where his work focuses on solving electromagnetic compatibility (EMC) challenges in mobile devices. His key responsibilities include the simulation and optimization of EMC performance for smartphones.

YOUNG PROFESSIONALS FORUM

VENUE	Liren Hall 2
TIME	12:00-13:00 November 6th
CHAIR	Syed Muzahir Abbas, Macquarie University, Australia Hanzhi Ma, Zhejiang University, China
INTRODUCTION	**Young Professionals Forum – Career Development and Growth Pathways** This session focuses on the professional development of young engineers, aiming to create an open and collaborative platform for sharing experiences and fostering mutual growth among early-career professionals. The discussion will revolve around three key topics: 1. **Establishing a Clear Career Vision** – How can young professionals define their long-term career direction and develop a practical roadmap for continuous growth in the early stages of their career? 2. **Developing Core Technical and Soft Skills** – What are the essential competencies that will shape the future of the electromagnetic and high-speed industries, and how can young engineers effectively enhance these skills to stay competitive? 3. **Building and Sustaining Professional Networks** – How can young professionals actively cultivate high-quality connections and leverage professional communities to accelerate their career advancement? Through sharing experiences, challenges, and success stories, this session encourages participants to explore actionable strategies for achieving sustainable professional development in the dynamic field of electromagnetics.

OVERVIEW OF IBIS SUMMIT

VENUE	Liren Hall 2
TIME	08:40-11:00 November 7th
CHAIR	Randy Wolff, Siemens EDA, USA Ling Zhang, Zhejiang University, China
INTRODUCTON	IBIS OPEN FORUM The IBIS Summit is an international technical forum organized by the IBIS Open Forum, bringing together experts and engineers in high-speed system design, signal integrity, and modeling to discuss the latest standards and technology trends. IBIS Summit China is one of its key regional events, attracting leading companies and research institutes across China every year. In 2025, for the first time, the IBIS Summit China will be concurrently held with the 2025 International Workshop on Advanced Interconnects (WAI 2025) in Ningbo, China. This strategic partnership is aimed to synergize the two communities, with a focused exploration of cutting-edge topics on high-speed interconnects, SI/PI, and chip-package EMC. The joint event is expected to bridge the gap between standardization, academic research, and industrial application, accelerating innovations for the future of AI.
INVITED TALK	**IBIS Chair's Report** *Doug Burns, SI-Clarity, USA* **IBIS Power Integrity Introduction** *Walter Katz, MathWorks and Arpad Muranyi, Siemens EDA* **IBIS 8.0: Specification and Parser Introduction** *Randy Wolff, Siemens EDA, USA* **IBIS Interconnect Task Group Update: Touchstone 3.0 Features & Progress** *Michael Mirmak, Intel, USA* **Efficient Time-Domain Noise Analysis Method** *Xiuqin Chu, Xidian University, China* **Conquer MIPI C-PHY Simulation Challenge** *Xiuguo Jiang, Keysight Technologies, China* **A Novel Physics-Assisted Genetic Algorithm for Decoupling Capacitor Optimization** *Ling Zhang, Zhejiang University, China*

HOW TO GET TO THE HUALUXE® NINGBO HARBOR CITY

Taking the Airplane

Ningbo Lishe International Airport →HUALUXE® Ningbo Harbor City

→ Enter Lishe International Airport Station (Line 2, toward Honglian).

→ Transfer at Gulou Station to Metro Line 1 (toward Xiapu)

→ Get off at Changjiang Road Station (Exit A1).

Taking the (High-speed) Train

Ningbo Station→HUALUXE® Ningbo Harbor City

→ Enter Ningbo Railway Station Metro (Line 2, toward Honglian).

→ Transfer at Gulou Station to Metro Line 1 (toward Xiapu).

→ Get off at Changjiang Road Station (Exit A1).

→ Walk 436 meters to reach HUALUXE Ningbo Harbor City.

Driving by Yourself

Please search for "HUALUXE Ningbo Harbor City" in GPS. The navigation will plan your traffic route according to your current position.

Parking: HUALUXE Ningbo Harbor City

ACCOMMODATION

Special rates have been negotiated for the 2025 WAI in Ningbo attendees at HUALUXE Ningbo Harbor City.

If you need to book a room, please contact the hotel before November 1, 2025, quoting the name of the conference to make a reservation at the special rate.

Hotel Name：

HUALUXE Ningbo Harbor City
宁波港城华邑酒店

Hotel Address：
No. 1199 Changjiang Road, Beilun District, Ningbo City, Zhejiang Province
宁波市北仑区长江路 1199 号

Hotel Phone Number：
+86 574-86799999

Recommendations for other hotels:

Hotel Name：

Hanting Hotel (Ningbo Beilun Changjiang Road Subway Station Branch)

Hotel Phone Number：
+0574-26881666

The venue can be reached from the hotel in 8 minutes on foot (599 meters).

Hotel Name：

Ningbo Meike City Hotel

Hotel Phone Number：
+ 0574-86863066

The venue can be reached from the hotel in 6 minutes on foot (445 meters).

Hotel Name：

Yaduo Hotel, Beilun Youth Sports Center, Ningbo

Hotel Phone Number：
+86 574-27629888
The venue can be reached from the hotel in 8 minutes by car (1.2 km).

ABOUT NINGBO

Ningbo, also known as Yong, is located halfway down the coastline of the Chinese mainland and to the south of the Yangtze River Delta. It is bordered by the natural bulwark of the Zhoushan Archipelago to the east, the city of Shaoxing to the west, the city of Shanghai to the north across the Hangzhou Bay, and the city of Taizhou and Sanmen Bay to the south.

The city's history can be traced back to the Hemudu Culture that originated 7,000 years ago. In the Xia and Shang Dynasties about 4,000 years ago, Ningbo was known as Yin. Later, in the Spring and Autumn Period (770-476 BC), it became part of the State of Yue. In the Qin Dynasty (221-206 BC), it encompassed Yin, Mao and Gouzhang, three areas under the Kuaiji Shire. In the Tang Dynasty (618-907 AD), it was named Mingzhou. In 821 AD, the local authority moved towards the junction of three local rivers and built city walls, marking the establishment of today's city. In 1381 AD, the city acquired its current name of Ningbo, or, literally, Calm Waves.